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An efficient procedure Of interfacing a Programmable logic controller with peripheral Unit

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ABSTRACT: *The key objective of this research is to illustrate an organized and efficient way to interface driver or Siemens S7 200 programmable logic controller (PLC) with load or BCD to seven segment decoderby implementing logics through ladder logic diagram (LLD). In this paper, we are presenting LLD program for reducingcounter delay time in PLC and propagation delay time in decoder inoperation of driver and loader together. This will make interfacingof this two electrical system efficient. This system will also provide noise immunity between driver and load by introducing effective noise margin compatible for both system.*
***Keywords**:Efficient interfacing, Interfacing, PLC, PLC with peripheral unit, Peripheral unit control by PLC*

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I. INTRODUCTION

It is undoubtedly admissible that technological advancement solely depends on novel ideas or concepts, paradigm shifts, integrations of two or more embedded or self-contained system and improvements in operational efficiency of existing design. The purposeful intermingling of two or more well-suited electrical, electronic or mechanical systemcan be a very challenging process because of their different functional characteristics. The logics, effectiveness and efficiency of interconnections always need to be experimentally correct. Hence, proper understanding of I/O characteristics of these modules and calculable interactive solutions within system have to be guaranteed.In this paper, SIEMENS SIMATIC S7-200 PLC, BCD decoder and interfacing of these two units are discussed with calculable solution for improving efficiency in operation when a communication is established between them.

II. PROGRAMMABLE LOGIC CONTROLLER:

Programmable logic controller (PLC) isa microprocessor based solid state member of computer familywhich stores instructions in programmable memory unit and executes commands according to input and functional LLD. The functions like- sequencing, timing, data manipulation and communication, counting, arithmetic etc. are the key features to control output processing unit. Technically, most of the time it replaces timers, counters and necessary sequential relays circuits to provide user a simple and practical operational environment. There are several models of PLC in the market now-a-days, like- PLC S-7 200, 300, 400, 1200, ET 200, TI 545, 555, SLC 500, Modicon 984 PLC, MicroLogix, PLC 5 etc. In thisillustration of interfacing procedure of a PLC with peripheral unit, we are going to use SIEMENS SIMATIC S7-200 model.

Figure 1:PLC trainer (SIEMENS SIMATIC S7-200 PLC inside)

Siemens PLC 200 trainer is a complete set of lab equipment which has a variety of I/O module and a micro programmable logic controller (Micro PLCs) - PLC S7 200 unit.It has CPU 221-224, 226 and CPU 224XP system. It also gets new memory cartridge support.It can execute Boolean logics, complex mathematical operations, LLD and can also communicate with other devices comfortably. Its features allow it to be both as a stand-alone Micro PLC solution and in concomitance with other controllers in functional process.

III. SEVEN SEGMENT DECODER UNIT:

Seven segment decoder unitis an IC which converts digital bits from one format to another. In seven segment display system, it converts binary coded decimal (BCD) bits into seven segment display decoder bits. The output of seven segment decoder is displayed in the process of electroluminescence by 7 segment light emitting diode (LED) display or Light Crystal Display (LCD).

BCD numbers are coded numbers of decimal digits. It is not a direct decimal to binary conversion of a number rather it takes every decimal digit of a number and converts it into its binary equivalent digits and presents all BCD bits of the number altogether. For example, a binary conversion of 123 is 01111011 while BCD code is 000100100011. BCD needs more bits to represent a number but it is less complex system than direct binary to decimal conversion.

Table of Decimal digits and its equivalent BCD:

Decimal number	BCD
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001

The 7 segment decoder needs complex arrangement of logic gates. Because it takes BCD input and sends output in the form of light in seven segment display (SSD) or seven segment indicator so that the user can understand the numerical value of a structure that it creates. In Figure 2, four input of 7 segment decoder are assigned as A, B, C and D and the outputs are a, b, c, d, e, f, and g which creates a decimal numerical structure in the electroluminescence procedure. This figure provides the basic circuit diagram and truth table of seven segment decoder.

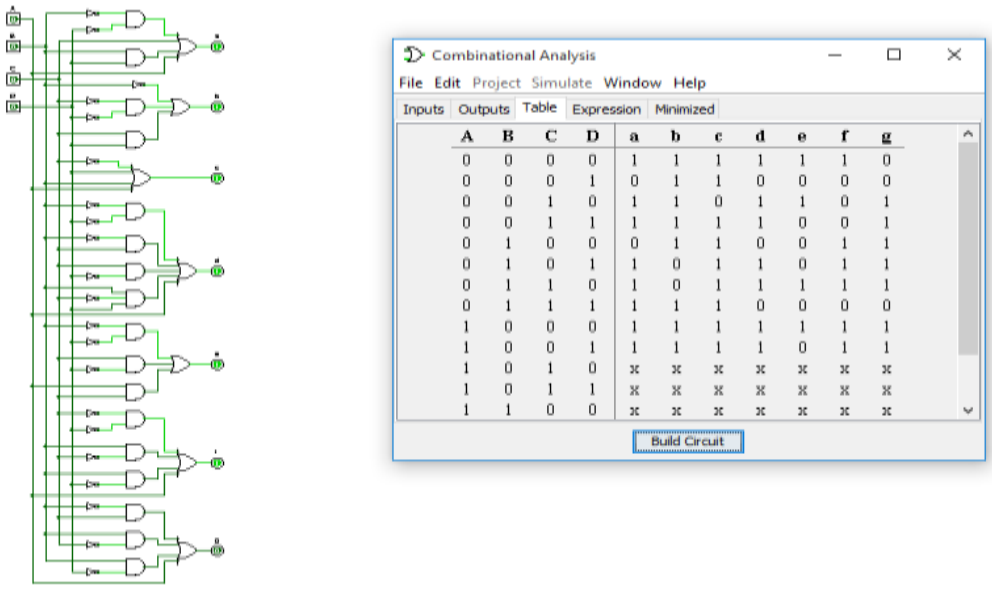


Figure 2: Circuit diagram and Truth table of BCD to seven segment decoder

This large circuit can be replaced by modern tiny silicon chip known as integrated circuit or IC. IC comprises of all kind of active and passive electronic components isolated by isolation diffusion within crystal chip.IC 7447 is one of the ICs which can convert BCD to 7 segment display digits. In Figure 3, Common cathode display, IC 7447(U1) and four voltage changing state unit (switch) are connected with each other via wire to display a numerical value. We know that, the BCD value 0100 is equivalent to 4. This conversion isdone successfully in this simulation. Practically, the operation of 7 segment decoder is same as the simulation in Figure 3.

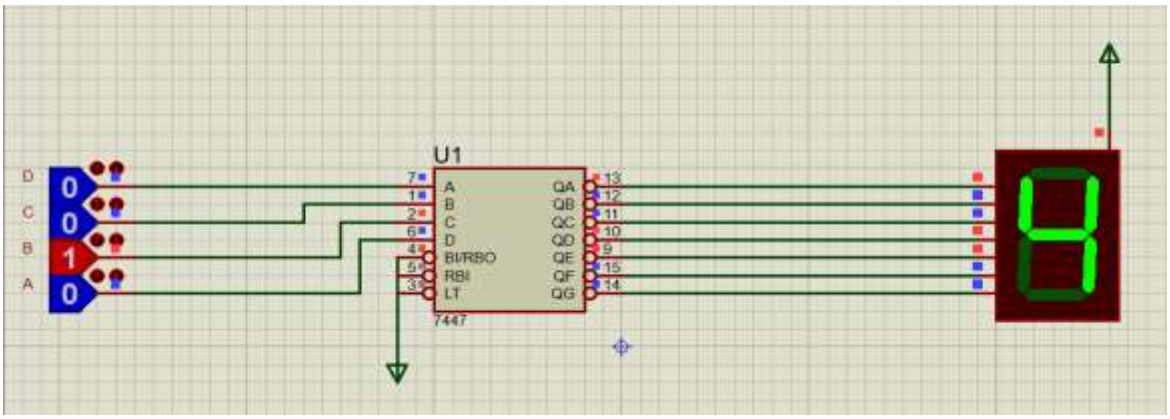


Figure 3: BCD to 7 segment decoding display simulation

IV. INTERFACING A PLC WITH 7 SEGMENT DECODER UNIT

Interfacing is a logical process of congregating two characteristically dissimilar electrical system or circuit so that the newly fabricated system can serve a particular purpose. PLC and 7 segment system both have their own functional IC. Interfacing of these units are nothing but a setup of logical communications between ICs. IC of PLC acts as driver which sendsdriver output voltage HIGH or LOW (signal) to load IC or 7 segment decoder. For successful interfacing, driver has to make sure that it should have such voltage levelwhich consistently keep load active at LOW or HIGH (0 or 1) state. It can be done by considering required load voltage and noise margin level.

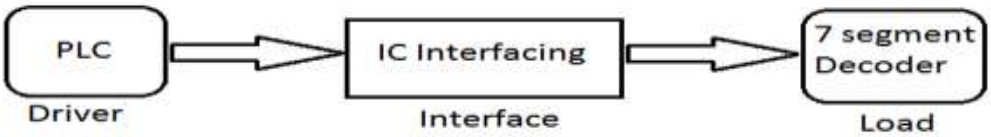


Figure 4: Basic diagram of interfacing a PLC system with 7 segment decoder unit

In Figure 5, driver voltage, $V_{DOVH\ (min)}$ and $V_{DOVL\ (max)}$shouldbe ensured the following level:
$V_{DOVH\ (min)} > V_{NH}+V_{LIVH\ (min)}$
And $V_{DOVL\ (max)} +V_{NL} < V_{LIVL\ (max)}$
Where, $V_{DOVH\ (min)}$ = Driver output voltage high (1), $V_{DOVL\ (max)}$ = Driver output voltage low (0), V_{NH}= Voltage at Noise level high, V_{NL}= Voltage at Noise level low, $V_{LIVH\ (min)}$=Load input voltage high (1), $V_{LIVL\ (max)}$= Load input voltage low (0)
These voltage level provides noise immunity in the interfacing process. PLC S7 200 IC maintains $V_{DOVH\ (min)}$ and $V_{DOVL\ (max)}$so that it can provide enough voltage $V_{LIVH\ (min)}$ and $V_{LIVL\ (max)}$for BCD decoder IC unit.

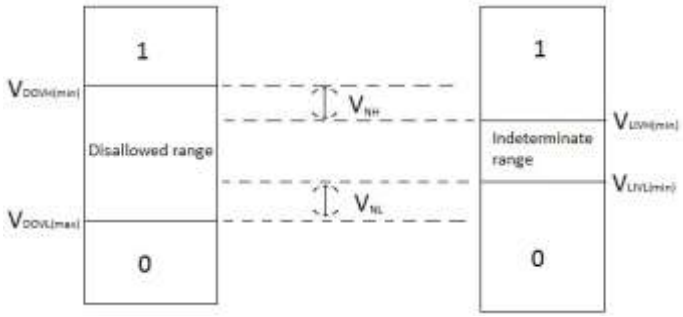


Figure 5: Noise margin level between driver and load

Additionally, interfacing efficiency depends on synchronous voltage state (0 or 1) change of driver and load. The simultaneous alterability of voltage state can be defines as speed in interfacing. The reduction of counter delay time in PLC and propagation delay time in BCD decoder rely upon the speed of interfacing, proper range of noise margin level, capability of command processing and suitable internal construction or design of a system. In figure 6, Siemens PLC S7 200 trainer's internal diagram of SSD unit with assigned PLC interfacing points are drawn. Manually, I0.2 to I0.5 are for digit change and I0.6 to I1.1 are for status change of digits.

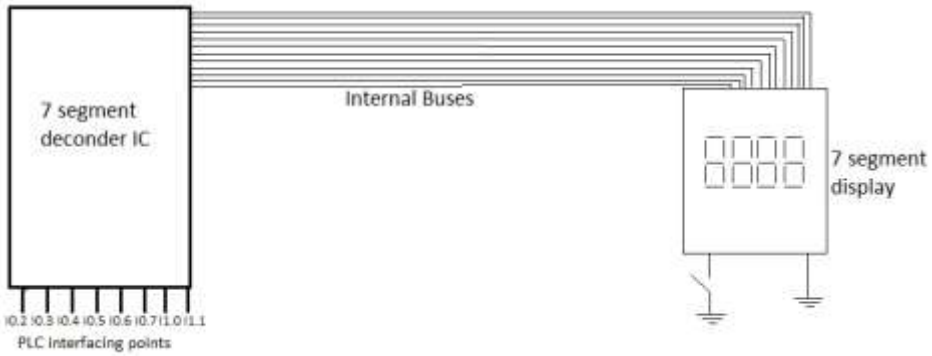
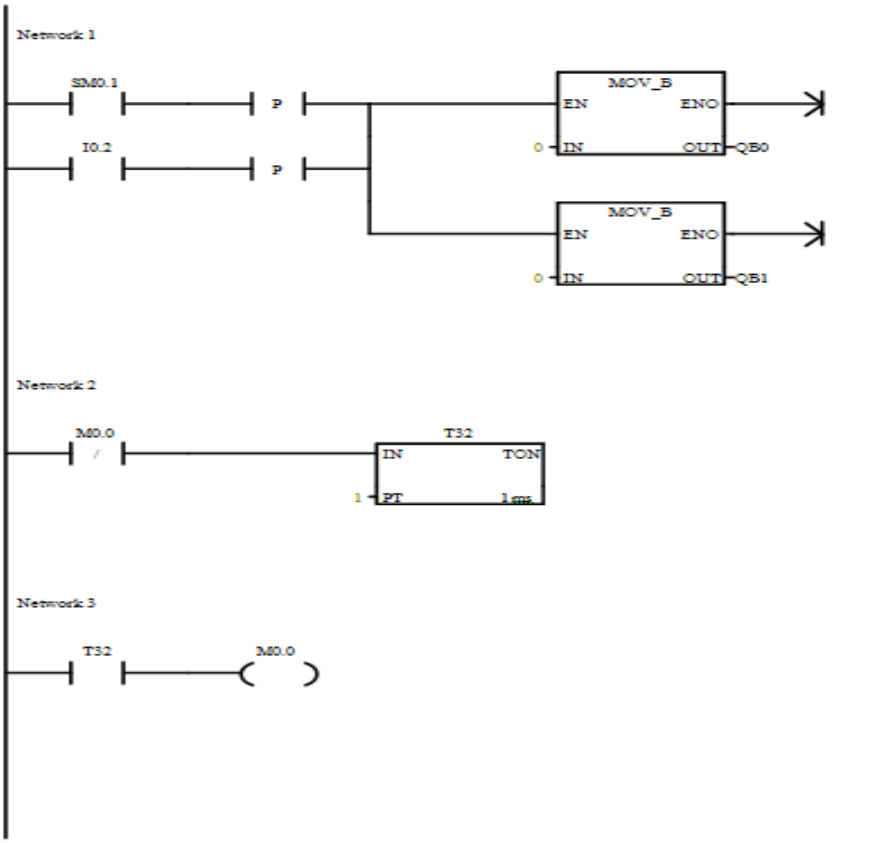
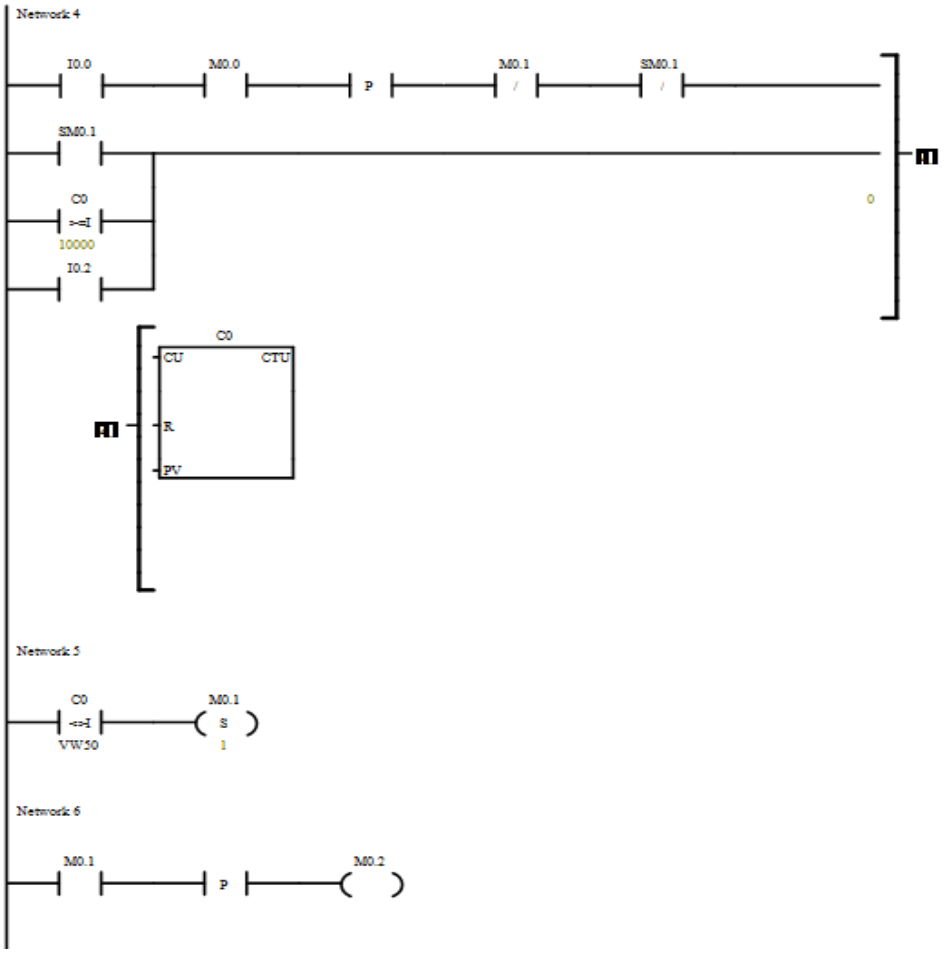


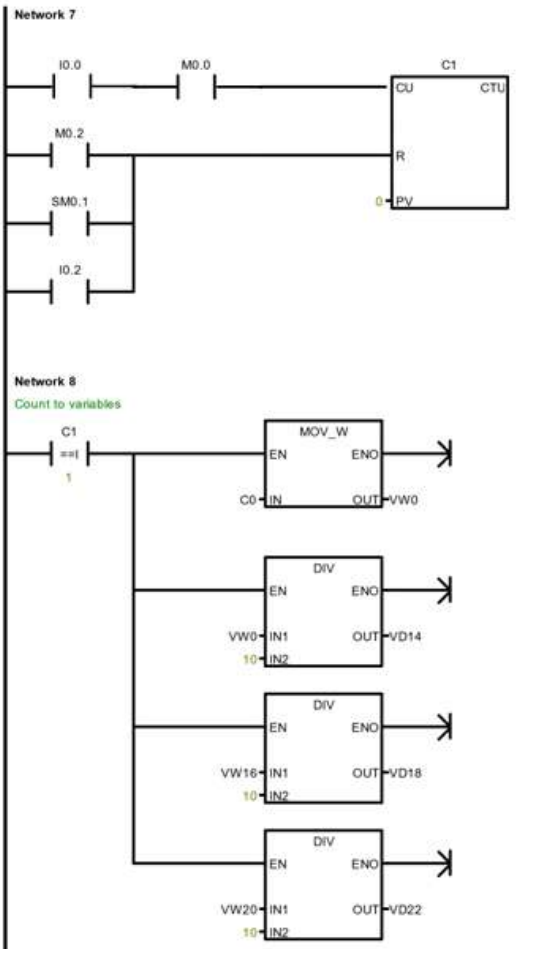
Figure 6: Internal diagram of build-in 7 segment decoder in Siemens PLC S7 200 trainer

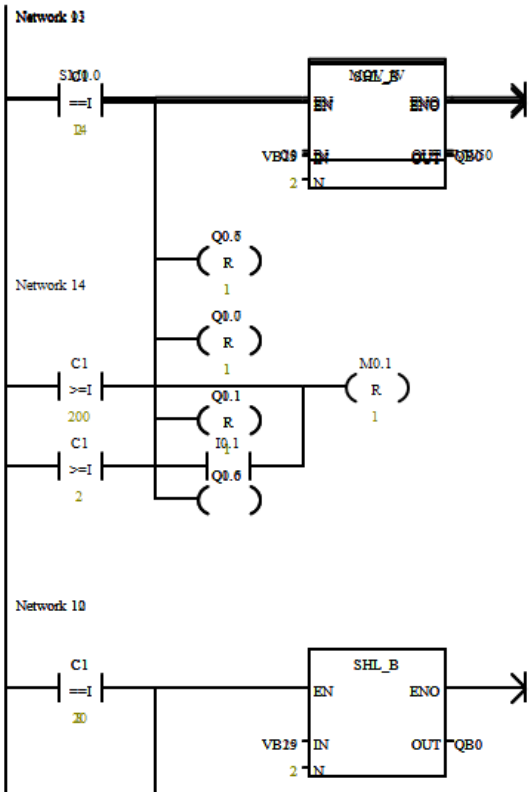
V. LLD AND ITSDESIGN OF EFFICIENT INTERFACING

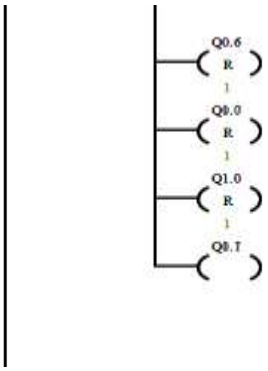
In this paper, we are designing a LLD for 4 digit output from seven segment display in which noise margin level is maintained by PLC IC and BCD decoder IC unit in operation. Without this level, our system will stop working or will provide us flawed counting. Now, the speed of interfacing needs to be fixed. The system will count from 0 to 9999. So, it requires maximum 16 bits to represent a number. It is know that QB0 and QB1 have in total 16 bits. When the use of QB0 byte will be finished, QB1 will start providing required bits.So, in network 1, for SM0.1 or first scan and positive transition (which allows power to flow for one scan for each on to off transition) or I0.2 ON state and positive transition take all the input to output byte in either QB0 or QB1. In Network 2 to 3, a clock is created by turningM0.0 ON and OFF with the help of T32 on delay timer. In network 4, the condition of I0.0, M0.0, M0.1, SM0.1 and positive transition makes C0 or counter run, up until 10000 or the range of counting in 4 digit display.Now the counting is needed to be shown in display unit. We need another counter to show our counting in display unit. So, C1 counter has to be activated and put into work for this reason. In network 5, counter reset condition is defined. M0.1 will be reseted within VW50 range. In network 6, M0.2 condition is set by M0.1 and positive transition. In network 7, I0.0 and M0.0 activate C1 which is different condition of turning C0 ON state. M0.2 condition is for reset C1. When M0.1 and positive transition simultaneously turned on C1 resets and starts working again. C1 counter determines which bits to show in display unit. Manually, if we turn on I0.6 to I1.1, we will actually turning on a digit in display. Q0.6 to Q1.1 replace I0.6 to I1.1. Now, if we need to show digit on display, we need to activate digit after certain times which is compatible for both IC. We have to choose a certain amount of time consciously so that both IC can interact with each other without any interruption effectively and efficiently. We choose 6ms difference in counter so that digits can appear without any internal fault in mechanism and program.Before that, we have to assign digits for Q0.6, Q0.7, Q1.0 and Q1.1. To choose that, we consider a variable memory unit VW0 which has 4 digit number. Suppose, VW0 has 1234. Now, if we divide it by 10, we will get 123.4 in VD14. VW14 and VW15 have remainder 4 and VB16 and VB17 have 123 as quotient. After that, VW16 or 123 is divided by 10 again and VD18 has 12.3. So, VB18 and VB19 have remainder 3 and quotient 12. Similarly, we get VD22=1.2 by dividing VW20 by 10. VB22 and VB23 have remainder 2 and quotient 1. All of this single digit 1, 2, 3 and 4 can be assigned in VB25, VB23, VB19 and VB15 memory bytes respectively. This operation is done in network 8 by C1 counter. In network 9-12, VB15, VB19, VB23 and VB25 variables are shifted to output with additional 2 unit and Q0.6, Q0.7, Q1.0 and Q1.1 are turned on one after another but not altogether. When Q0.6 is on, then rest of bits are off. Same thing happens for rest of the bits. The digits appear in the display are saved in memory. 2 unit added as I0.0 and I0.1 are used by other commands. C0 counter feeds as input and output VW50 which will set M0.1. C1 counter will not reset up until 200ms. If we donot set C1 as 200ms, we will not be able to watch the number in counter due to high speed. These two operation are done in network 13 and 14. Now, if this program is run from PC, it will be able to count the number and the interfacing will be effective and efficient.


Network 1
SM0.1
P
I0.2
P
MOV_B
EN
ENO
0
IN
OUT
QB0
MOV_B
EN
ENO
0
IN
OUT
QB1
Network 2
M0.0
T32
IN
TON
1
PT
1 ms
Network 3
T32
M0.0


Network 4
I0.0
M0.0
P
M0.1
SM0.1
SM0.1
C0
>=I
10000
I0.2
0
C0
CU
CTU
R
PV
Network 5
C0
<=I
VW50
M0.1
S
1
Network 6
M0.1
P
M0.2


Network 7
I0.0
M0.0
C1
CU
CTU
M0.2
R
SM0.1
0
PV
I0.2
Network 8
Count to variables
C1
==I
1
MOV_W
EN
ENO
C0
IN
OUT
VW0
DIV
EN
ENO
VW0
IN1
OUT
VD14
10
IN2
DIV
EN
ENO
VW16
IN1
OUT
VD18
10
IN2
DIV
EN
ENO
VW20
IN1
OUT
VD22
10
IN2


Network 13
Network 14
C1
>=I
200
M0.1
R
1
Q0.1
R
I0.1
C1
>=I
2
Network 10
C1
==I
SHL_B
EN
ENO
VB19
IN
OUT
QB0
2
N



VI. RESULT

The developed LLD program is now installed in PC with the help of V4.0 STEP 7 MicroWIN SP9 program. Now, when we have run the proagram, we have found that seven segment display showing number which counts from 0 to 9999 without any interruption. In Figure 8, we have showed the real time example of the execution of the LLD.

Figure 8: System test result after implementing LLD

From this result, we are ensured that there were no interruption of voltage between two IC which means a successful interfacing is done and noise immunity has been established by ICs.

After checking different time variables, we found that if counter C1 provide s 6ms difference to turn any digit ON, it becomes more efficient and successful. This time difference reduces counter delay time in PLC IC and propagation delay time in decoder IC in operation.The speed of PLC IC is swifter than speed of BCD decoder IC. So, PLC IC have to wait 6ms to ensure successful and efficient interfacing with BCD decoder IC. Otherwise, the system losesitsefficiency.

VII. DISCUSSION AND FURTHER RESEARCH

In this paper, an efficient way of interfacing SIMATIC S7-200 PLC with seven segment decoder unit are discussed with LLD. Practical result of this LLD implementation for improving efficiency of interfacing and reducing propagation delay time and counter delay time is also illustrated. Noise immunity between ICs is ensured as well. In this LLD design, second counter (C1) must have to wait 6ms to get synchronized with BCD decoder IC.From this experiment, we can conclude that, in SIMATIC S7-200 PLC system, 6ms PLC IC waiting time provides efficient interfacing between PLC and seven segment unit or peripheral unit.

In the future, we will try to analysis I/O characteristics of other type of electrical system to integrate that with PLC and will develop LLD for efficient and effective use. Besides, we will try to utilize state-of-art

technology for minimizing complexity in LLD and will try to do graphical analysis of our developed LLD program performance in operation.

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