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Optimum design of phase opposition disposition pulse width modulation logic circuit for switching seven level cascaded half bridge inverter

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ABSTRACT: *Theevolution of multilevel inverters (MLIs) has made it possible to extract power from direct current (DC) sources to alternating current (AC) power. This paper presents the design of a novel phase opposition disposition pulse width modulation scheme (PODPWM) logic circuit for a conventional single phase seven level cascaded H-Bridge (CHB) inverter using Matlab/Simulink. The minimum switching logic circuit for the single phase seven level CHB inverter was obtained by modeling the logic equations that could be used with any number of levels depending on the number of modulating and carrier signals involved. The reduction in total harmonic distortion (THD) of the output voltage for the MLI using low switching frequency at different modulation indixes is also investigated. The logic equations have made it easier to design a PODPWM circuit for any CHB inverter and the logic gates designed gave an optimum THD value of 16.73 % at modulation index of 0.20.*

Keywords-*CHB, Matlab, MLI, PODPWM, THD*

I. Introduction

The increase in energy production from fossil fuel sources is to meet the ever increasing demand for power. But there is enormous pressure to reduce global warming which is one of the demerits of fossil fuel energy production. Thus, the use of inverter technology to exploit renewable energy sources has been introduced. However, conventional inverters have limitations at high power and high voltage applications [1]. This has made multilevel inverter (MLI) more popular for high power and high voltage applications due their increased number of levels at the output. As the number of level increases, the harmonics are reduced and output voltage tends to be more pure [2].
Multilevel inverters have switching regulators which could be Bipolar Junction Transistors (BJTs), MOSFETs or Insulated Gate Bipolar Transistor (IGBT) through which the output voltage levels can be controlled. Pulse width modulation techniques are normally employed for switching MLIs.

The aim of this paper is to design a logic circuit that uses phase opposition disposition (POD) strategy to control a single phase seven level cascaded H-bridge inverter. The paper establishes equations for the design of logic modulation circuit for any number of levels for a cascaded H-bridge inverter using PODPWM and also investigates the best amplitude modulation index at which significant reduction in total harmonic distortion could be achieved.

II. Principle of Operation

The conventional seven level cascaded H-bridge inverter comprises twelve switches which form three half bridges (H bridges). The three half bridges have cascaded connection. Each H- bridge has a separate DC voltage source with three levels (+Vdc, 0,-Vdc), so the output voltage levels in the seven level CHB inverter are (+3Vdc, +2Vdc, +Vdc, 0,-Vdc,-2Vdc,-3Vdc) [3]. In this paper, the signals to the switches of the single phase seven level MLI are modulated using PODPWM. The modulation technique involves the sampling of six carrier signals to produce the seven output voltage levels. The modulating or the reference signal has the frequency $f_m$and an amplitude A_m while the carrier signal has the frequency f_c and an amplitude A_c. At each instant, the carrier signals are compared with the reference signal to give the desired output.

III. Basic Seven Level CHB Inverter

The modulation strategy for an inverter involves two parameters called amplitude modulation index or ratio (m_a) and frequency modulation index or ratio (m_f).These indixes are obtained from the various parameters that contribute to the efficiency of the inverter [4].

For m-level cascaded H-bridge multilevel inverter, the amplitude modulation index and frequency modulation index [5] are given as:

$$m_a = \frac{A_m}{(m-1)A_c} (1)$$

$$m_f = \frac{f_c}{f_m} (2)$$

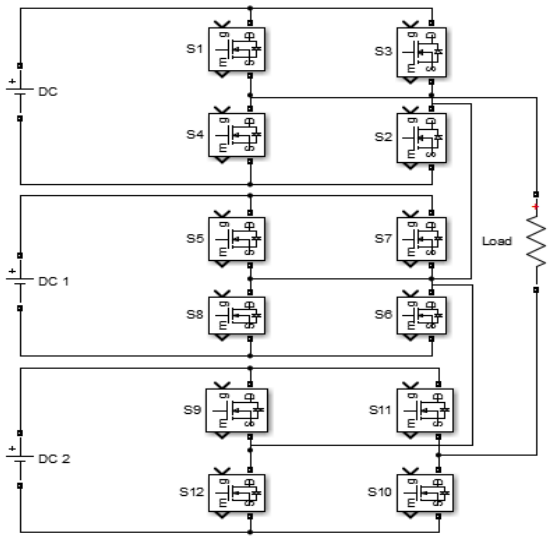

Figure 1.Conventional seven level CHB inverter

IV. Multicarrier Pulse Width Modulation

The carrier modulation schemes for MLIs are divided into two categories: phase-shifted and level-shifted multi carrier modulations [6]. Both modulation schemes can be applied to the cascaded H-bridge inverters. The THD value of phase-shifted modulation is higher than level-shifted modulation [7]. The level shifted multicarrier modulation scheme is categorized into four: phase opposition disposition (POD) method, alternate phase opposition disposition (APOD) method, phase disposition strategy (PD) and inverted phase disposition (IPD). In phase opposition disposition method, all the carrier waveforms above zero reference are in phase but they are 180° out of phase with the carrier signals below it. Alternative Phase Opposition Disposition (APOD) PWM has each carrier band shifted by 180° from the adjacent bands. Phase disposition (PD) PWM is similar to APOD except the carriers are in phase [8]. In inverted phase disposition scheme, all the carrier waveforms are inverted and intersected with the modulating waveform. When the modulating signal is higher than all the six carrier waveforms, pulses are generated in upper sequence and when the modulating wave is lower than all the six carrier signals, pulses are generated in the lower sequence [9]. Anuradha, Mohit and Suman [10] show that the THD of phase voltage of asymmetrical seven level cascaded multilevel inverter (CMLI) is studied under different modulation methods such as PD, POD and APOD and the least THD of 17.72 % is observed for APOD. Therefore, POD which has the highest THD value of 18.05 % is chosen for the inverter so that the THD value of the output voltage could be observed with the use of XOR and XNOR logic gates. The switching logic table for the MLI is shown in Table1.

Table 1. Table to Switch the Seven Level Inverter

S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	Voltage level
1	1	0	0	1	1	0	0	1	1	0	0	+3vdc
1	1	0	0	1	1	0	0	1	1	1	1	+2vdc
1	1	0	0	1	1	1	1	1	1	0	0	2+vdc

1	1	1	1	1	1	0	0	1	1	0	0	+2vdc
1	1	0	0	0	0	0	0	0	0	0	0	+vdc
0	0	0	0	1	1	0	0	0	0	0	0	+vdc
0	0	0	0	0	0	0	0	1	1	0	0	+vdc
1	1	1	1	1	1	1	1	1	1	1	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	1	1	1	1	1	1	1	1	-vdc
1	1	1	1	0	0	1	1	1	1	1	1	-vdc
1	1	1	1	1	1	1	1	0	0	1	1	-vdc
0	0	1	1	0	0	1	1	1	1	1	1	-2vdc
0	0	1	1	1	1	1	1	0	0	1	1	-2vdc
1	1	1	1	0	0	1	1	0	0	1	1	-2vdc
0	0	1	1	0	0	1	1	0	0	1	1	-3vdc

V. MODELING OF SWITCHING LOGIC EQUATIONS

The operation of a traditional single-phase seven level cascaded H-bridge inverter requires six carrier signals and a modulating waveform which combine to produce pulses that switch the inverter using PODPWM. The switches of the CHB inverter are numbered from S_1 *to* S_{12}. The logic equations based on the analysis of the combination of the reference and the carrier signals are modeled but in order to reduce the propagation delay time and number of gates for implementation, De Morgan's laws are applied to the equations which give rise to the simplified equations below:

$$S_1 = A \oplus G \quad (15)$$

$$S_4 = \overline{A \oplus G} \quad (16)$$

$$S_5 = A_1 \oplus G \quad (17)$$

$$S_8 = \overline{A_1 \oplus G} \quad (18)$$

$$S_9 = A_2 \oplus G \quad (19)$$

$$S_{12} = \overline{A_2 \oplus G} \quad (20)$$

$$S_3 = B \oplus G \quad (21)$$

$$S_2 = \overline{B \oplus G} \quad (22)$$

$$S_7 = B_1 \oplus G \quad (23)$$

$$S_6 = \overline{B_1 \oplus G} \quad (24)$$

$$S_{11} = B_2 \oplus G \quad (25)$$

$$S_{10} = \overline{B_2 \oplus G} \quad (26)$$

Where A,A_1,A_2,B, B_1, $B_2$and G are signals that produce pulses for the inverter.

VI. Logic Gate Based PODPWM

The phase opposition disposition circuit is designed based on the switching pattern of the twelve switches in the conventional single phase seven level cascaded H-bridge inverter. The logic circuit is based on the modeled equations and it is made up of AND, OR, and NOT logic gates. But to simplify the circuit, XOR and XNOR logic gates are used for implementation.

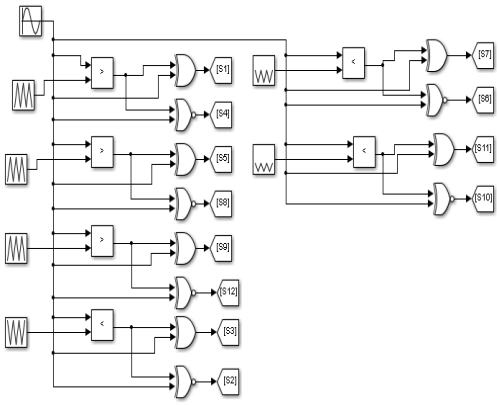

Figure 2. PODPWM logic circuit for seven level CHB inverter

VII. Simulation Results

Simulation of the gate-based PODPWM circuit for the traditional seven level CHB inverter is performed using Matlab software. The DC voltage used for each of the three half bridges of the inverter is 100V. The output voltage waveforms are generated at the carrier signal frequency of 5 KHz and at the frequency modulation index of 100.

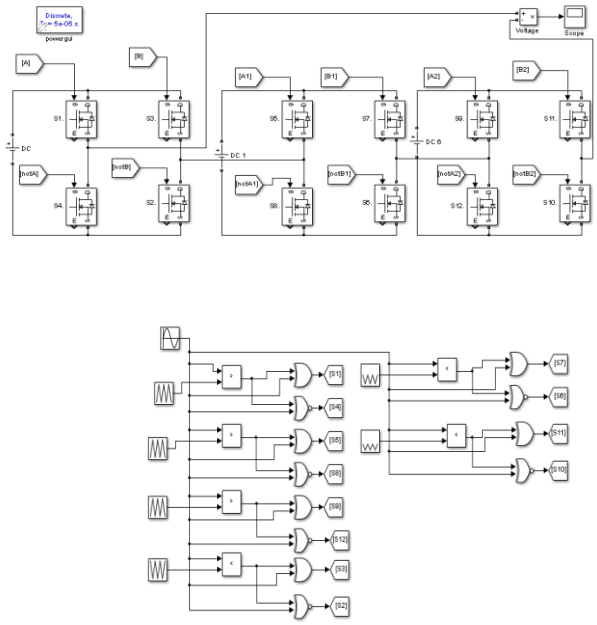

Figure 3. Seven level CHB inverter with logic gate circuit

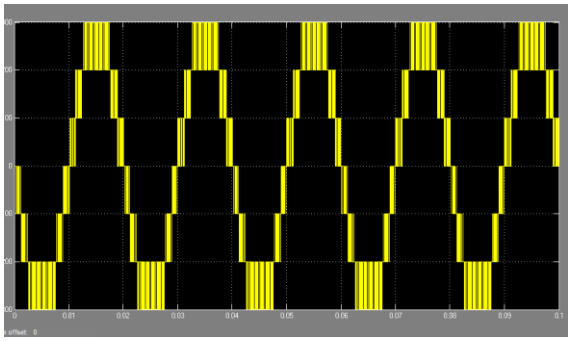

Figure 4. Output voltage waveforms of the inverter at m_f=100

The simulation is also done at amplitude modulation indices ranging from 0.10 to 0.24 at an interval of 0.02 to determine a relative decrease in THD value of output voltage around $\frac{1}{6}$ (≈ 0.17), which is a parameter value of amplitude modulation index when PODPWM is used for seven level inverter.

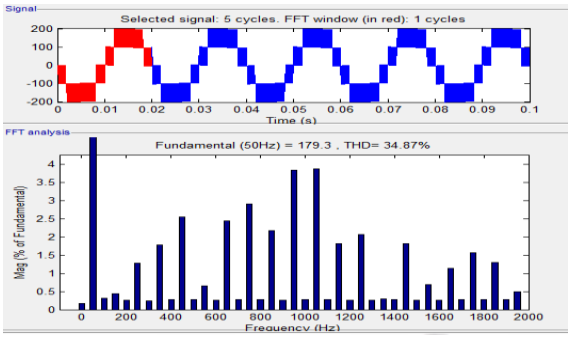

Figure 5. Output voltage waveform and THD spectrum at m_a=0.1

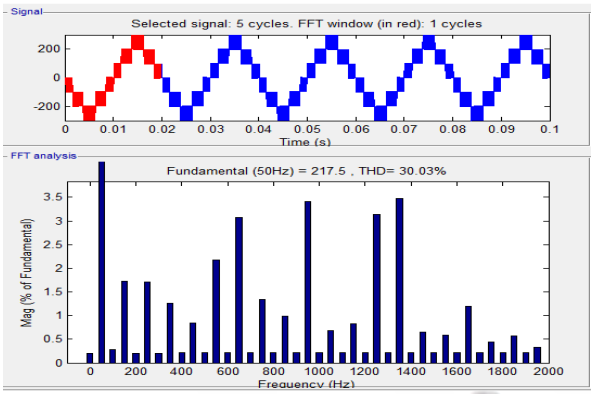

Figure 6. Output voltage waveform and THD spectrum at m_a=0.12

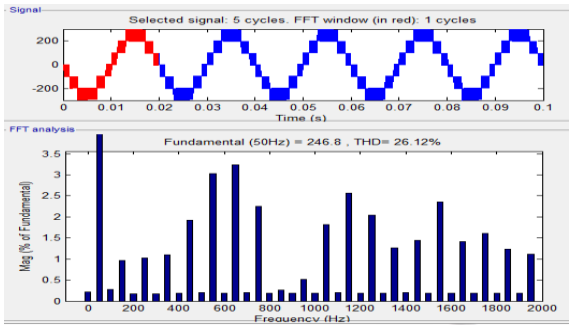

Figure 7. Output voltage waveform and THD spectrum at m_a=0.14

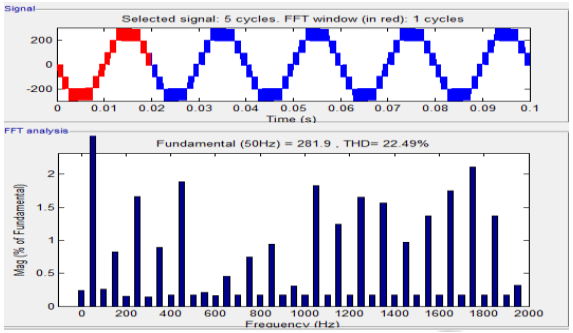

Figure 8. Output voltage waveform and THD spectrum at m_a=0.16

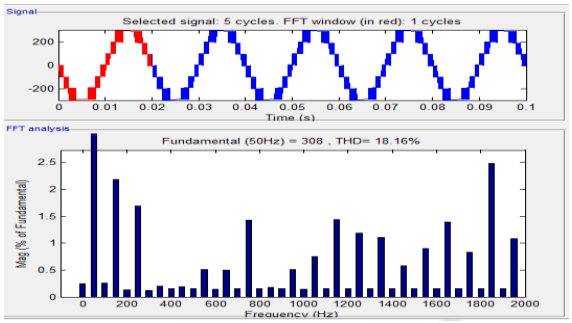

Figure 9. Output voltage waveform and THD spectrum at m_a=0.18

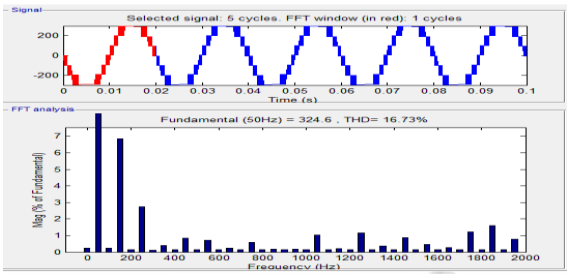

Figure 10. Output voltage waveform and THD spectrum at m_a=0.20

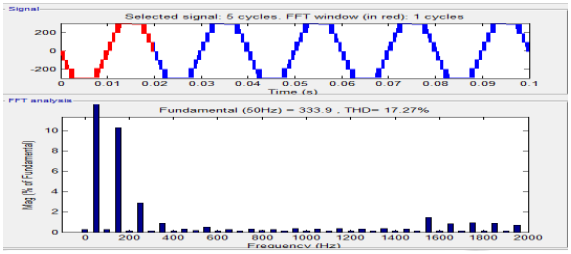

Figure 11. Output voltage waveform and THD spectrum at m_a=0.22

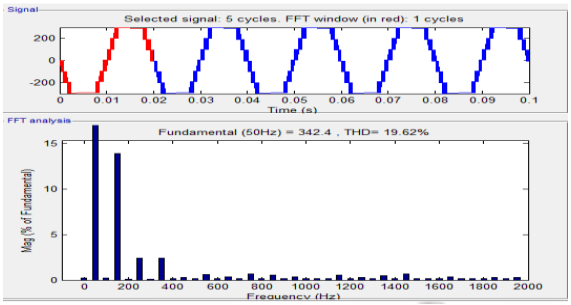

Figure 12. Output voltage waveform and THD spectrum at m_a=0.24

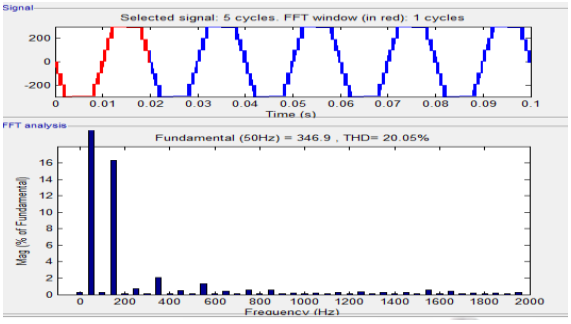

Figure 13. Output voltage waveform and THD spectrum at m_a=0.26

The THD values at different amplitude modulation indices are summarized in Table2.

Table 2. THD Values at Different Modulation Indices

Modulation Index	THD value (%)
0.10	38.87
0.12	30.03
0.14	26.12
0.16	22.49
0.18	18.16
0.20	16.73
0.22	17.27
0.24	19.62
0.26	20.05

VIII. Conclusions

The proposed PODPWM logic gate circuit uses six XOR and six XNOR gates based on the derived equations to produce pulses for the seven level MLI. The logic equations have made it easier to design a modulation circuit for a CHB inverter with any number of levels using PODPWM. The THD value of the output voltage for the proposed modulation circuit at the carrier frequency of 5 KHz around $\frac{1}{6}$ (≈ 0.17) amplitude modulation index is found to decrease steadily with increase in the modulation index from 0.10 to 0.20, where the least THD of 16.73 % is achieved without the use of a filter. However, the THD value increases gradually with increase in modulation index from 0.22 to 0.26. Therefore, the proposed logic circuit can be implemented at amplitude modulation index of 0.20 where the relative decrease in THD value is of prime importance.

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