American Journal of Engineering Research (AJER) 2015
American Journal of Engineering Research (AJER)
e-ISSN: 2320-0847 p-ISSN : 2320-0936
Volume-4, Issue-12, pp-95-100
www.ajer.org
Research Paper Open Access

Efficient carry skip Adder design using full adder and carry skip block based on reversible Logic

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Abstract: *In recent years, Reversible Logic is becoming more and more prominent technology having its applications in Quantum Computing, Nanotechnology, and Optical Computing. Reversibility plays an important role when energy efficient computations are considered. In this paper, binary full Adder with Design I and Design II are proposed. The performance analysis is verified using number of reversible gates, Garbage input/outputs, delay, number of logical calculations and Quantum Cost. According to the suitability of full adder design I and design II carry skip adder block is also constructed with some improvement in terms of delay in block carry generation. It is observed that Reversible carry skip Binary Adder with Design II is efficient compared to Design I.*
Keywords-*Fenyman gate, Fredkin gate, Reversible carry skip adder, Garbage Input/output, Quantum Cost*

I. INTRODUCTION

1.1 ***Reversible logic***

Reversible computing was started when the basis of thermodynamics of information processing was shown that conventional irreversible circuits unavoidably generate heat because of losses of information during the computation [5]. The different physical phenomena can be exploited to construct reversible circuits avoiding the energy losses. One of the most attractive architecture requirements is to build energy- lossless small and fast quantum computers.

A Reversible circuit/gate can generate unique output vector from each input vector, and vice versa, i.e., there is a one to one correspondence between the input and output vectors. Thus, the number of outputs in a reversible gate or circuit has the same as the number of inputs, and commonly used traditional NOT gate is the only reversible gate. In digital design energy loss is considered as an important performance parameter. Part of the energy dissipation is related to non-ideality of switches and materials. Landauer's [1] principle states that irreversible computations generates heat of K×Tln2 for every bit of information lost, where *K* is Boltzmann's constant and T the absolute temperature at which the computation performed. Bennett [2] showed that if a computation is carried out in Reversible logic zero energy dissipation is possible, as the amount of energy dissipated in a system is directly related to the number of bits erased during computation.

Since adders, subtractors [11], multipliers [8] are the important blocks for the computation and if these are designed using reversible gates, information loss in computation can be prevented up to the extent of feasibility of circuit based on reversible logic.

1.2 ***Carry skip adder***

In traditional carry skip adder design an adder block of multiple full adders is constructed. These adder blocks along with carry skip block can be combined to make a carry skip adder to add any number of binary bits.

This adder block receives input carry signal and provides output carry signal .This input carry signal may ripple through each stage of the adder block and appear at the output or it can be predicted by using carry skip block. The carry skip block predicts the intermediate carry output of each stage (full adder) of the adder block on the basis of a carry propagate signal. If carry propagate signal of first stage is one input carry propagate to next stage (full adder) as well as if all the propagate signals are one the input carry is propagated to the output. If any or all propagate signal is zero, input carry signal is not transferred to the output in this case the carry generated

after addition process in last stage is transferred to the output. The propagate signal of each stage in adder block is connected to an AND gate to provide block propagate signal .Now this block propagate signal is combined with the carry output of final stage by using an OR gate to generate final carry output. Figure 1 shows the 4 bit carry skip adder block.

The carry skip worst case delay is observed when the carry generated in very first full adder, ripples through each full adder stage in first block .Thus carry output generated by the first block skips all the intermediate blocks and then it ripple through the full adder stages of the last block[6].

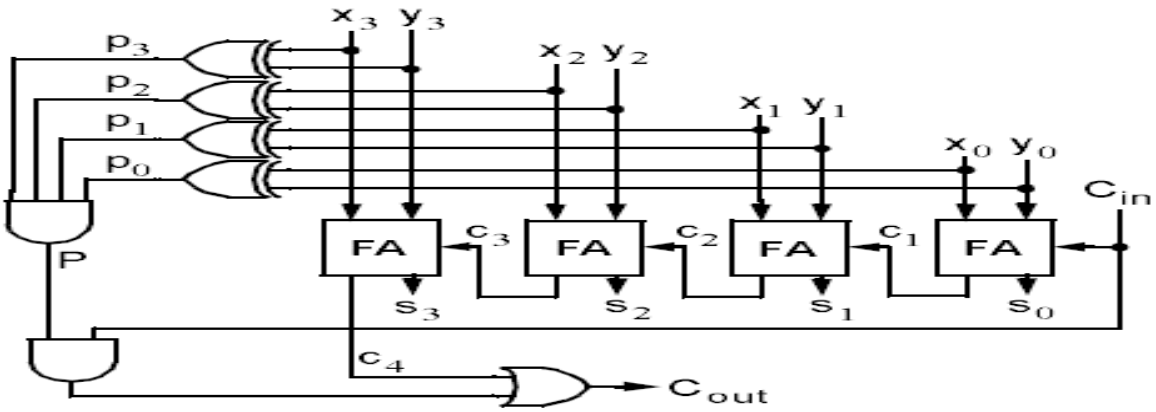

Figure1

II. BASIC REVERSIBLE LOGIC GATES

There are many reversible logic gates to perform reversible operation. These gates can be used to achieve desired output and optimization of the circuit. To achieve optimization in reversible circuit one should not allow any Fan-out and Loops or feedbacks along with this Garbage outputs, delay and quantum cost should be minimized. These reversible gates can perform various operations in different input conditions. This paper includes 2 basic reversible gates which are as follows.

2.1 Feynman(F) / CNOT Gate

The Fenyman gate is also called Controlled NOT (CNOT) gate it is 2 inputs and 2 gates as shown in Figure 2. This gate maps the input (X_1, X_0) to output $Y_1 = Y_0$ $Y_0 = X_1 \oplus X_0$ Quantum Cost of Fenyman gate is one [8]. It can also be used to generate fan out signal by keeping one input to ground according to Figure 3.

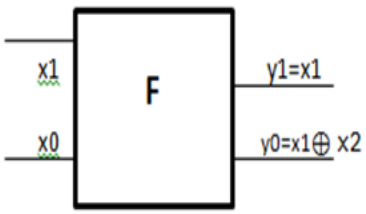

Figure 2

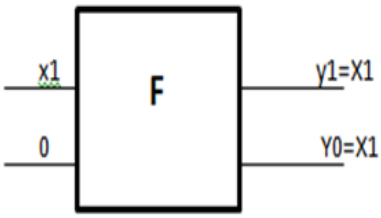

Figure3

2.2 Fredkin Gate (FG)

The Fredkin gate shown in Figure 4 is a Reversible 3×3 gate which maps inputs (X_2, X_1, X_0) to outputs $Y_2 = X_2$, $Y_1 = X_2X_1' + X_2X_0Y_0 = X_2X_1' + X_2X_0'$ .Its Quantum cost is 5[8]. The FG can be used to choose any one of the 2 inputs by applying control signal.

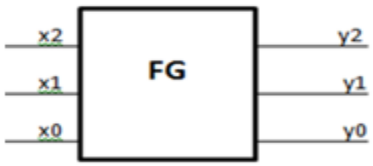

Figure4

$\mathbf{Y_2=X_2}$

$$\mathbf{Y_1}=\begin{bmatrix} X_1 & Y_2=0 \\ X_0 & Y_2=1 \end{bmatrix} \qquad \mathbf{Y_0}=\begin{bmatrix} X_1 & Y_2=1 \\ X_0 & Y_2=0 \end{bmatrix}$$

The FG gate can also be used to create the inverse and fan out function as in Figure5 [4]. 2 input AND gate can be generated by grounding one terminal as in Figure 6[4]. The 2 input OR gate can be generated by tying one terminal of FG to supply voltage according to Figure 7. Higher order AND and OR logic can be realized by using FG arranged in Binary tree .A B bit requires B-1 FGs. An input passes a maximum of $log_2 N$ FGs.

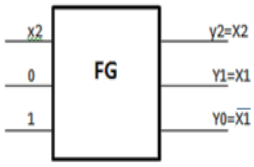

Figure5

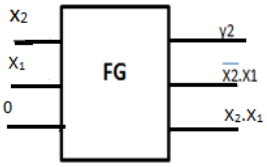

Figure6

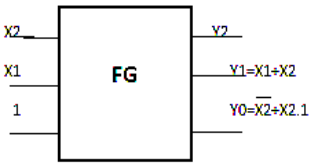

Figure7

III.PROPOSED MODEL

The Reversible gates such as F and FG are used to construct Design I and Design II full Adder. These design are applied to make carry skip adder. Further some delay improvement is also done in carry skip block by determining the state of each propagate signal one by one.

3.1 Design I

This design shown in Figure 8 represents one bit full adder which includes one fenyman gate (F) and 4 fredkin gate (FG).Fenyman gate provides the XOR operation of x1 & y1.The first FG is used to generate 2 signals x1⊕ x2 and complement of $X_1 \oplus X_2$.further if C_{in} is one the sum is $X_1 \oplus X_2$ and if C_{in} is 0 sum is $\overline{X_1 \oplus X_2}$.In each case sum and its complement appears at the output of this FG. On the basis of these signals, it can be decided that the value of C_{out} is $x1+C_{in}$ and $X1.C_{in}$.The total delay in generation of sum signal appears to be one F and 4 FG delay but as in [6] sum bit is the control bit to the 4th FGs hence the delay becomes to be equal to 3 FGs delay. The propagate signal is generated after the one F and one FG delay. This is faster than the design in [6].C_{in} is control bit in one FG but it transferred at the output after 2 FG delay , since it depends upon the sum and its complement hence total delay in generating C_{out} is one F and 4 FG. There are 2 constant input 3 garbage output and total quantum cost 21 along with total transistor count in design 22where design of fenyman gate includes 6 transistors and transistor used in FG design is 4[10] however the Verilog code for Fredkin gate used in this design includes 6 transistors.

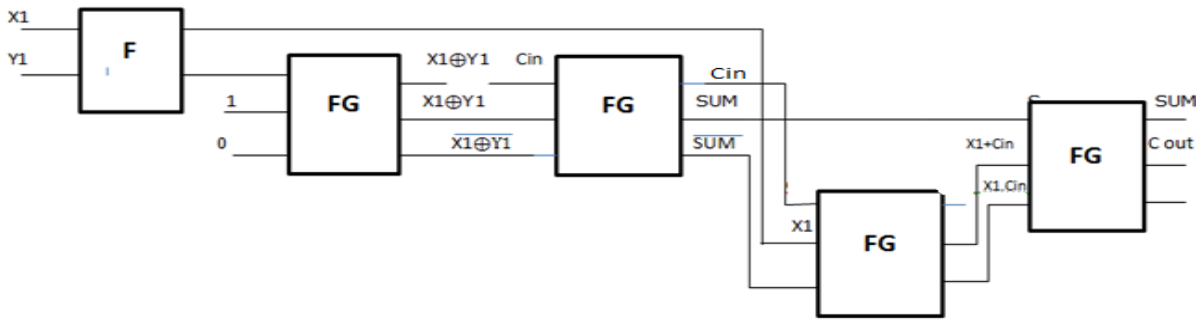

Figure8

3.2 Design II

As shown in Figure 9 proposed design II, 4Fs and 2 FGs are used. The sum is generated after 2 Fenyman gate and its complement is generated by using 1fenyman gate with 1input at logic 1. The propagate signal is generated after 2 F gate. Similar to design I carry is generated after sum signal hence the delay in C_{out} generation is 3 Fs and 2 FGs. Quantum cost of the design is 14. The garbage outputs are 3 and constant inputs are 2.

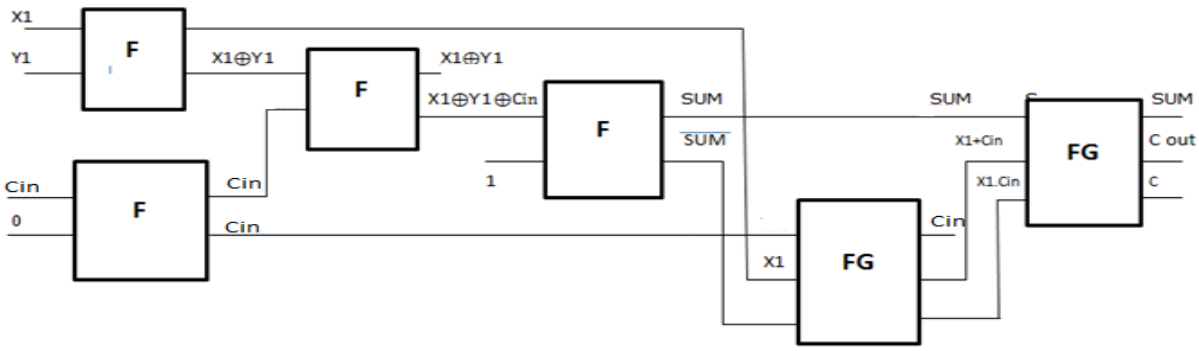

Figure9

3.3 Reversible 4bit carry skip Binary Adder

The Figure10 shows the circuit of carry skip adder block to add 4 binary bits. Add operation is performed by full adder due to any one of design I and design II. The AND -OR gate of carry skip block of Figure 2 is replaced by the fredkin gate carry skip logic. In this circuit instead of performing AND operation the fredkin gates provide decision making one by one to each carry propagate signal of each full adder. If first propagate signal is one, second propagate signal is examined and when it appears logic 1, AND operation is performed between last two propagate signal. Thus this design can avoid the delay in AND operation when either first or second or both propagate signals are 0.The total quantum cost of carry skip adder block for 4-bit adding operation is 76.The constant inputs are 11 and garbage bits are 19.

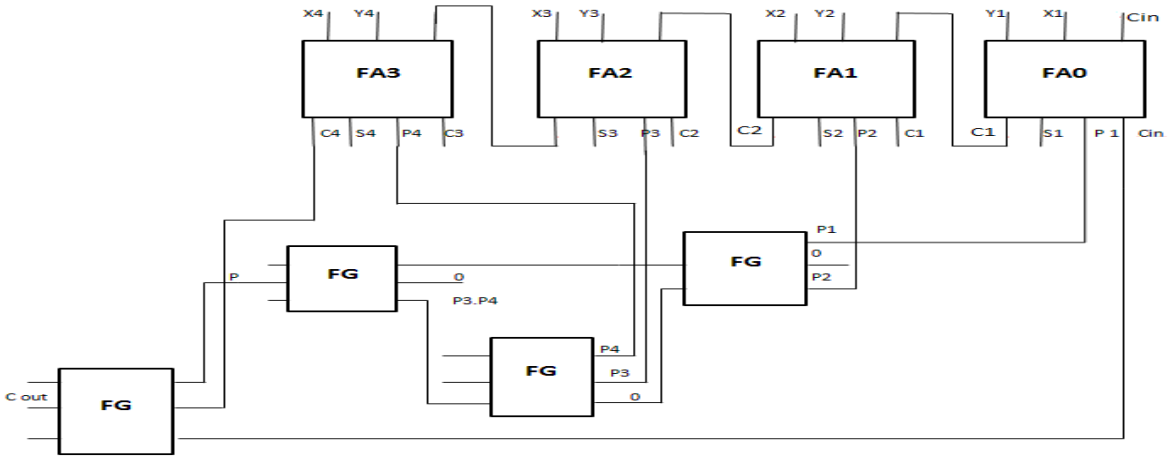

Figure10

To construct N bit adder these full adder block of B number of bit can be used. For worst case delay in output carry (C_{out}) generation it can be considered that the carry ripples in first and last B bit adder block and in all remaining B bit adder block delay in carry skip block is considered. In carry skip block worst case delay can be considered that all the propagate signals are one so delay of each FG in carry skip block can be considered. Total delay in carry generation in first and last B bit block is 2B per FG of carry transfer, delay of 2F in XOR operation of first two bit in each adder and carry of an adder stage also depends upon sum of previous stage so B F delay is included for final block carry generation. Hence total delay in first block is $2B\ FG + (B + 2)F$ as well as Delay in carry skip block is $\{(N/B) - 2\}$ 3FGs.

Hence worst case delay can be given as $T_{Carry} = 2\{3B\ FG + (B + 2)F\} + \{(N/B) - 2\}\ 3FG$

IV.RESULTS

4.1 Reversible Full Adder

Since number of transistor used in fenyman gate are 6 and transistor implementation of fredkin gate uses 6 transistors so the table 1 is sufficient to compare both the design.

Table I

Sr.No	*Design*	*Quantum cost*	*No. Of Transistor*	*Garbage output*	*Constant input*
1	I	21	36	3	2
2	II	14	36	3	2

Table II

Sr.No.	Design	Carry delay	Propagate signal Delay	Sum Delay
1	I	1F+4FG	1F+1FG	1F+2FG
2	II	3F+2FG	2F	3F

4.2 Reversible 4-bit carry skip Adder

The reversible carry skip full adder block for 4 bit is designed using the design II and some improvement in carry skip calculation is also done. The carry skip block receives first propagate signal P1and if this signal is one the propagate signal P2 is examined otherwise block propagate signal is set to logic zero value. The product of propagate signals P3 and P4 is taken on the basis of P1and if all the propagate signals are one the block propagate signal is generated. On the basis of propagate signals the decision of carry output is performed.

Table III

Sr.No	*Design*	*Quantum cost*	*No. Of Transistor*	*Garbage output*	*Constant input*
1	4 bit- carry skip Adder	76	152	19	10

Table IV

Sr.no.	*Design*	*Carry(worst case)*	*Propagate signal*
1	4 bit- carry skip Adder	$2\{3B\ FG + (B+2)F\} + \{(N/B) - 2\}\ 3FG$	2F

4.3 Simulation

Figure 11 shows the simulation waveform for each input combination of proposed full adder design I using Modelsim PE student edition 10.4

Figure11

Corresponding to proposed full adder design II the simulation waveform is shown in Figure 12.

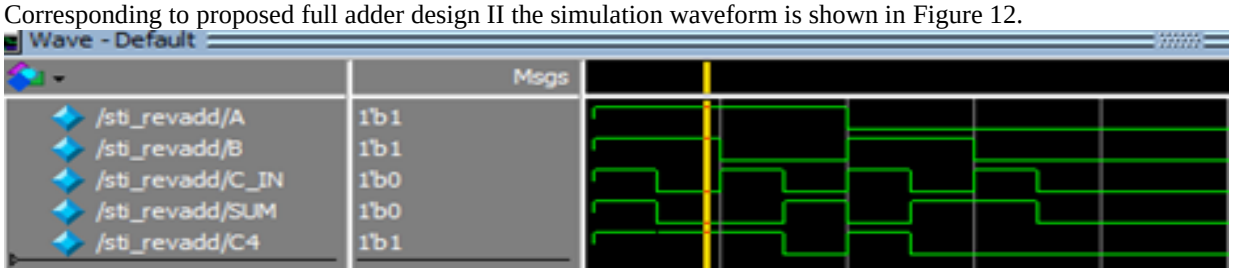

Figure12

Carry skip adder simulation result is shown in Figure 13, it is clear that when the block propagate signal (PR) is one, carry input (C_IN) propagates to the carry output (C_out) otherwise the ripple carry (C4) will be the carry output.

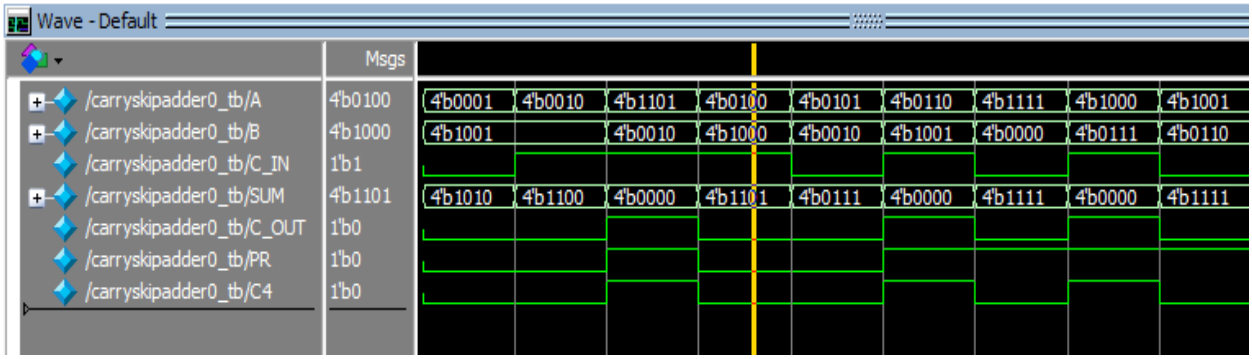

Figure13

V. CONCLUSIONS

Design I and design II both include the basic calculation of AND, OR and EXOR gate using reversible logic. The garbage count, number of transistor and delay are same for both the design but design II is better in point of view of quantum cost. The carry skip block also has some delay improvement over existing design because it checks the propagate signal of each full adder one by one hence reduces the delay in further calculations. The garbage output and constant inputs are reduced in carry skip adder block. In future, the design can be extended to any number of bits for Parallel Binary Adder & Subtractor unit and also for low power Reversible ALUs, Multipliers and Dividers.

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