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Design of a Low Voltage low Power Double tail comparator in 180nm cmos Technology

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ABSTRACT: *The need of analog to digital converters with ultra low power, area efficient and high speed is giving more chance to the use of dynamic regenerative comparators to maximize the speed and power efficiency. In this paper, an analysis on the delay and power of the dynamic comparators will be presented and based on the presented analysis, a new dynamic comparator is proposed, in which the conventional double tail comparator is modified for low power and fast operation even in small supply voltages. Here by adding a few transistors, the power consumptions can be reduced drastically. Post–layout simulation using 180nm CMOS technology confirms the analysis results of the proposed dynamic comparator.*

INDEXTERMS: *Double tail comparator, Power gating technique, Low-power analog design, Tanner EDA tool.*

I. INTRODUCTION

Comparators are the basic buildings elements for designing modern analog and mixed signal systems. A comparator compares the voltages that appears at their input and outputs a voltage representing the sign of net difference between them. For a comparator, speed and power consumptions are two important factors which are required for high speed applications like signal testing, sense amplifiers, data links, ADC etc. High speed comparators while implementing in ultra deep sub micrometer (UDSM) CMOS technologies faces the difficulty of lower supply voltages[1]. As CMOS technology reduces the size of the device smaller and smaller, the supply voltage also gets reduced to avoid the excessive field in the device.

So that, in order to avoid the conflict between the CMOS technology and comparator supply voltage either the threshold voltage of the comparator has to be scaled at the same pace as the supply voltage of the modern CMOS technology or boosting the supply voltages to the comparator requirements. Many methods like employing body driven transistors, supply boosting methods, using dual-oxide processes and current mode design is developed to meet the low voltage design challenges[2]. Boosting and bootstrapping techniques based on augmenting the supply, reference, switching problems and clock voltage, to address input range are effective methods, but implementing them in UDSM CMOS technologies introduced the reliability issues[3].
The threshold voltages requirement by the comparator can be reduced by implementing the body driven technique in the way that body driven MOSFET operates as a depletion- type device. But the body driven transistor suffers from smaller trans conductance compared to its gate-driven counterpart[4].

Apart from all these technological modifications, creating new circuit structures without stacking too many transistors is good for low voltage operations, if it does not increase the complexity of the circuit. According to the methodology, the conventional dynamic comparator can enhance the speed in low supply voltages by adding additional circuitry. Which adding the additional circuitry there arise the problem of component mismatch which effect the performance of the comparator[5]. A solution to this problem leads to the designing of double tail comparator, in which a separate input and cross coupled stage has been developed. And this enables a fast operation over a wide common-mode and supply voltage range[6].

Considering the delay a new dynamic double tail comparator was developed, which does not require boosted voltage or stacking of too many transistors, which resulted in the strengthening of positive feedback during regeneration. In this paper, based on the conventional double tail comparator as proposed previously, a new dynamic comparator is presented, which reduce power consumption drastically by using the power gating technique. By adding a few minimum size transistor to the conventional double tail comparator the power consumption can be reduced profoundly[7].

II. PROPOSED DOUBLE TAIL COMPARATOR

Clocked regenerative comparators can make fast decisions due to the strong positive feedback in the regenerative latch which helps them to find wide applications in many high speed ADCS. Based on different aspects like noise, offset, random decision errors and kick-back noise, several comprehensive, analysis have been presented recently. The working and operation of conventional single tail comparator and the double tail comparator has been presented earlier [8]. From the power and delay analysis study of these regenerative comparators, the proposed double tail comparator has been developed.

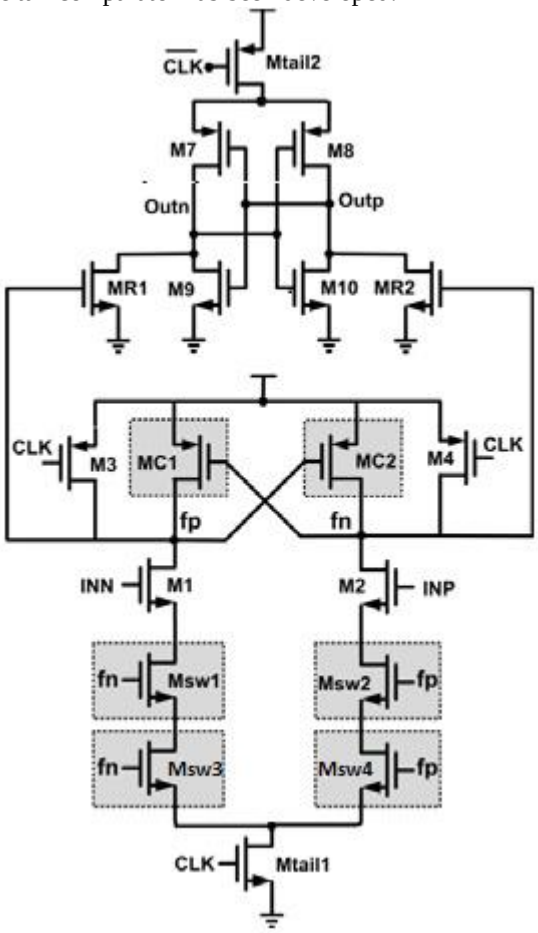

Fig. 1. Schematic diagram of Proposed double tail comparator.

A. *Operation of the Proposed Double Tail Dynamic Comparator*

The main idea of these comparator structures is to increase the voltage difference (ΔVfn/fp). In order to increase the latch regeneration speed two control transistors are added in parallel to M_3 and M_4 transistors in a cross coupled manner. About the operation of this comparator, during the reset phase, when CLK = 0, M_{tail1} and M_{tail2} is off and M_3 and M_4 transistors are on. And these transistors pull fn and fp nodes to VDD and M_{C1} and M_{C2} control transistors are in off stage. When fn and fp nodes get charged, the M_{R1} and M_{R2} intermediate transistors reset both latch output to ground. During the decision phase, when CLK = VDD, M_3 and M_4 transistors are off, M_{tail1} and M_{tail2} transistors are on and the control transistors are still in off condition. During this phase, the fn and fp nodes starts to discharge with different rates depending on the input voltages if VINP > VINN, then fn drops faster than fp which causes the corresponding PMOS control transistor (M_{C1}) starts to turn on, pulling fp node back to VDD. But the advantage of this structure is that, the other control transistor (M_{C2}) remains off and allowing fn to be discharged completely. In this comparator structure the difference between fp and fn has increased in an exponential manner. As soon as the comparator detects the fn node discharges faster, a PMOS

transistor (M_{C1}) turns on and node fp get charged to VDD. Irrespective of all these advantages, this structure helps to reduce the static power consumption. To overcome the static power consumption issue, four NMOS transistors are used below the input transistor. But the issue still continues as the leakage current is not completely stopped by using this technique. That means, the switching transistor cannot completely reduce the leakage current where VDD is drawn to ground via input and tail transistor (eg.M_{C1}, M_1 and M_{tail1}) which resulting in static power consumption.

III. MODIFIED DYNAMIC DOUBLE TAIL COMPARATOR

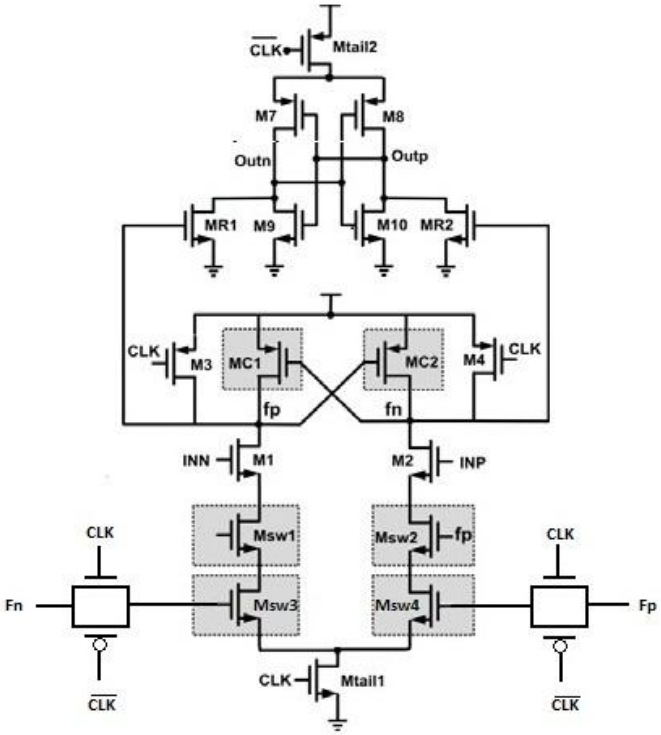

Fig. 2. Schematic diagram of the modified dynamic double tail comparator.

As the proposed double tail comparator architecture shows better performance in low voltage applications, the modified comparator is designed based on the double tail structure. The main idea of the modified comparator is to reduce the static power consumption by completely cutoff the flow of leakage current to the ground. For this purpose, two more switching transistors (M_{SW3} and M_{SW4}) have been added to the M_{SW1} and M_{SW2} transistors in a parallel manner using power gating technique. Here the modified structure can reduce the power consumption drastically.

B. Operation of the Modified Comparator

During the reset phase, when CLK = 0, M_{tail1} and M_{tail2} are off, M_3 and M_4 transistors get on and charge the fp and fn nodes to VDD during this time M_{C1} and M_{C2} are cutoff. Then M_{R1} and M_{R2} intermediate stage transistors reset latch outputs to ground. During the decision making phase, when CLK = VDD, M_{tail1} and M_{tail2} are on, M_3 and M_4 transistors turn off. At the beginning of the phase the M_{C1} and M_{C2} control transistors are still off (since fn and fp are about VDD). According to the input voltage fn and fp nodes starts discharging with different rates. If VINP > VINN ,then fp node discharge faster than fn, which causes the M_{C1} transistor turn on and recharge the fp node to VDD and M_{c2} will continue to be in off condition. So the voltage difference between fn and fp increases, leading to reduction of latch regeneration time. In the proposed idea, as one of the control transistor(eg.M_{c1}) turns on, a current form VDD is drawn to ground through M_{C1}, M_1, M_{SW1} and M_{tail1} which leads to static power consumption. Even the switching transistor M_{SW1} cannot completely reduce the flow of current and solve the static power consumption problem. Solution to the problem is adding two more NMOS switches below the switching transistors (M_{SW1} and M_{SW2}). Using the power gating technique in which domino logic style is implemented. During the decision phase, fn and fp nodes get discharged to ground depending on the input voltage, if INP > INN then fn node discharge faster than fp, which causes the M_{C1} control transistor to turn on and charge the fp node again and make the voltage difference faster. In order to maintain the fp node in charged condition and fn node discharged to ground, the switching transistors M_{SW1} and M_{SW2} are used, where M_{SW1} works

as a open switch as it got the input from fn node and M_{SW2} works as a closed switch, which helps in discharging the fn node completely to ground. In the proposed structure, two more switching transistors (M_{SW3} and M_{SW4}) with power gating technique and domino logic style has been used. This structure supports to pull the fp node up to VDD and discharging the fn node completely. This is possible as both the switching transistor M_{SW1} and M_{SW3} will be opened, at the same time M_{SW2} and M_{SW4} work as closed switches. In this structure power gating technique and using of domino logic style reduce the overall power consumption.

IV. SIMULATION RESULTS

In order to compare the proposed comparator with the single tail comparator and the conventional double tail comparators, all circuits have been simulated in 180 nm CMOS technology, VDD = 0.8v. Tanner EDA Tool is a leading provider of easy to use, PC based electronic based design automation (EDA) software solution for the design, layout and verification of analog – mixed signal integrated circuits. The result is simulated in T-SPICE platform and the circuit has been drawn using S-EDIT and got the output waveform in W-EDIT. Using the Tanner EDA Tool each comparator circuits has been simulated and got the output waveforms, which show the corrective working of the designed circuits. T-SPICE gives the power consumption and delay analysis results.

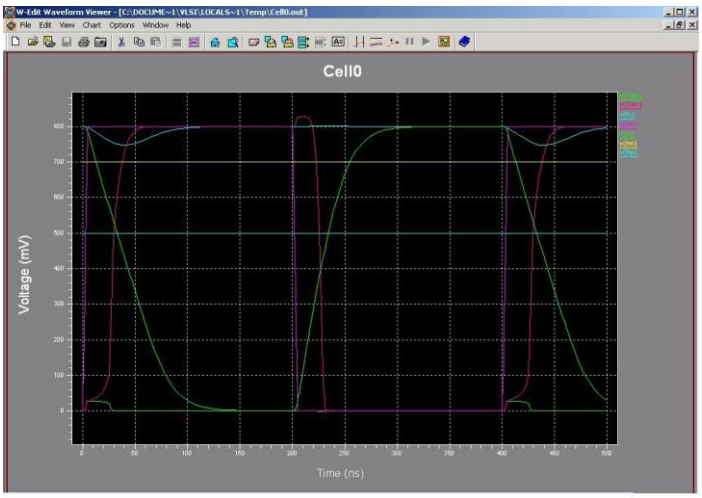

Fig. 6. Simulated output waveform of Proposed double tail comparator with INN = 0.5v, INP = 0.7v and VDD = 0.8v

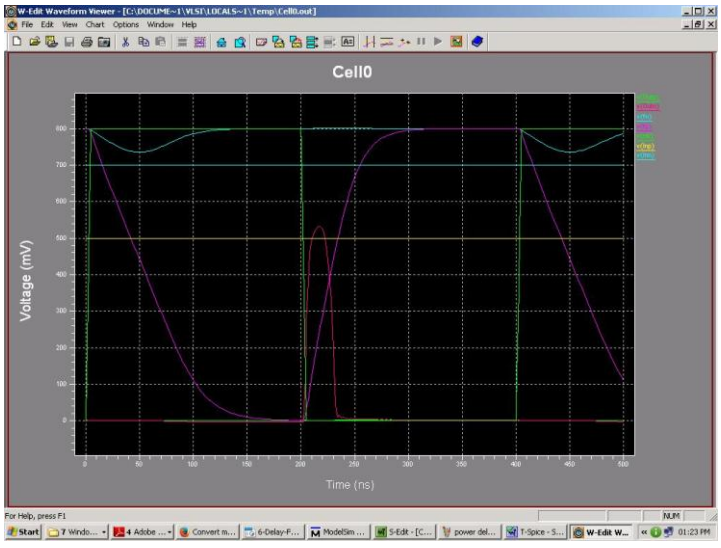

Fig. 7. Simulated output waveform of Modified double tail comparator.

For the simulation of all comparator structures, the supply voltage (VDD) given is 0.8v, the input voltage INP given is 0.7v and INN given is 0.5v. For each circuit structures the number of transistors used varies. The simulation results shows that for the proposed double tail comparator, the power consumption is reduced drastically when comparing all other comparator structures.

TABLE 1 PERFORMANCE COMPARISON

Comparator Structure	Single Tail Comparator	Conventional Double Tail Comparator	Proposed Double Tail Comparator	Modified Double Tail Comparator
Technology CMOS	180 nm	180 nm	180 nm	180 nm
Supply voltage (v)	0.8v	0.8v	0.8v	0.8v
Power Consumption (watts)	7.04×10^{-6} watts	1.50×10^{-5} watts	1.29×10^{-5} watts	9.50×10^{-6} watts
Delay (sec)	6.61×10^{-8} sec	7.51×10^{-9} sec	7.48×10^{-9} sec	4.84×10^{-9} sec

V. CONCLUSION

In this paper, a comprehensive analysis of power and delay for clocked dynamic comparators were done. Based on the analysis, a new dynamic double tail comparator with low voltage, low power capability was proposed to improve the performance of comparator, mainly concerned in power consumption. Post layout simulation results in 180 nm CMOS technology confirm that the power consumption of the proposed comparator is reduced to a great extent in comparison with all other dynamic comparators.

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