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Balanced and Unbalanced Input Voltage Harmonic Reduction in the Distribution Network Using Space Vector Pulse Width Modulation

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ABSTRACT: *Harmonic reduction caused by balanced and unbalanced input voltage in the distribution network was considered in this work. Space Vector Pulse Width Modulation (SVPWM) was adopted as switching signal generation. The algorithm of the developed SVPWM was written with Matlab codes in Matlab function block for Switching signal calculation rather than assembling various Matlab blocks to improve the simulation time and response time. Under balanced input voltage condition, the developed SVPWM achieved a reduction of THD of 0.91% as compared to 25.60% prior to compensation on inductive loads. In addition, the developed SVPWM model was compared with and without compensation under unbalanced input voltage and the result shows that the developed SVPWM achieved reduction in THD of 1.74% as compared to 26.68% after and before compensation. The developed SVPWM model was also compared with SPWM under balanced and unbalanced input voltage condition. The results show that SVPWM performed better than SPWM. All the results obtained are within IEEE 519 harmonics standard (i.e. THD less than 5%) with inductive loads under balanced and unbalanced voltage.*

KEYWORDS: *Harmonics; SVPWM; Unbalanced input Voltage; Inductive Loads*

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I. INTRODUCTION

The quality of supply voltage has been given a significant attention in recent time. Unbalanced input voltage in the electrical distribution network is one of the power system disturbances that pose a threat to power quality in power system engineering [1]. Voltages imbalanced are when the utility supply in the three-phase distribution system are not the same. The most common causes of unbalanced input voltages are imbalanced utility supply; tap settings of transformer tap not the same, loads unequal e.t.c [9]. This unbalanced input voltage increases the total harmonics distortion in the distribution and also degrades the power quality of supply [3]. The longetivity of electrical machines, electrical equipment and household electrical appliances are diminished which leads to significant economic losses in term of revenue [4].

The conventional harmonic reduction is a passive power filter and easy way to reduce the harmonic current. However, the capability of Passive power filter to remove all the harmonic distortion at the point of coupling (PCC) is limited. Some of the setbacks are bulkiness and frequency resonance with the grid inductance, therefore increases the harmonics distortion [19][6].

In recent times Active Power Filters (APF) was introduced and accepted as one of the most common compensation method. APF makes use of power electronics device to control the switching states of the inverters for harmonic cancellation at PCC so that harmonics free load current is supply to the consumers at PCC [5]. The strategies use to obtain the reference signal, method for switching signal generation and inverter DC voltage determine the effectiveness of shunt active power filter (SAPF) [9].

Synchronous Reference Frame (SRF) theory widely used for reference signal generation owing to its directness, accuracy and flexibility when compared to other methods [1].

Space Vector Pulse Width Modulation (SVPWM) is known for its complexity and higher with rigorous mathematical calculation for switching signal generation [10].

This work presents balanced and unbalanced input voltage reduction in harmonic in the distribution system. Synchronous reference frame is used for reference signal generation. Space Vector Pulse Width

Modulation (SVPWM) is used for switching pulse generation. The paper is arranged as follows: section one introduce the concept of the work, section two details the mathematical model of the developed model. Section three explains the design procedure and implementation, while section four present the results and discussed of the obtained results and section five details the conclusion of the work.

II. SHUNT ACTIVE POWER FILTER (SAPF)

The goal of SAPF is to reduce harmonic current and to improve the power factor that is caused by consumption of reactive power in the power supply [24]. The shunt active power filter works by feeding the exert harmonics current extracted in the opposing direction to the grid at PCC. The achievement of active power filter hinged on the method used to generate reference current and the switching method used to control the inverter legs [8]. The block diagram of SAPF is shown in Figures 1.

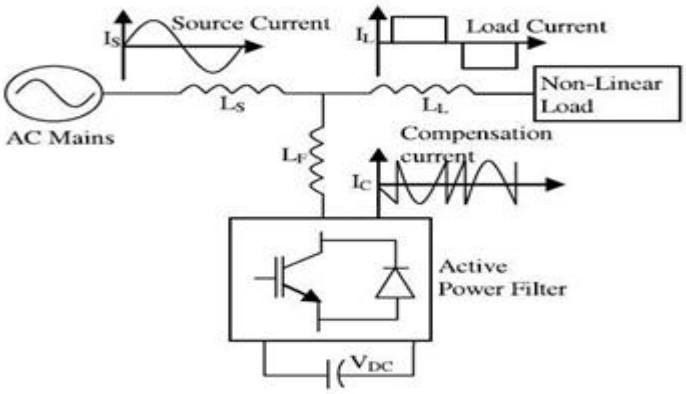

Figure 1: Block diagram of a SAPF [2]

A. Synchronous Reference Frame (d-q)

The d-q theory transforms three phase voltage and current in a-b-c quantities into d-q in dc quantities [11]. It transforms from a-b-c to (α-β) using Clark transformation equation and then transform from (α-β) to (d-q-0) using park transformation equation [12].

$$\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos\theta & \cos(\theta - 2\pi/3) & \cos(\theta + 2\pi/3) \\ -\sin\theta & -\sin(\theta - 2\pi/3) & -\sin(\theta + 2\pi/3) \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (1)$$

B. Concept of Space Vector Pulse WidthModulation

Space vector pulse width modulation consists of six actives sector and two non-actives sector with reference voltage vector $\vec{V}_{ref}$ which moves round the states vector.

The diagram of a three-phase bridge inverter is shown in the Figure 3. The upper transistors S_1, S_3 and S_5 determine the current output voltage [13].

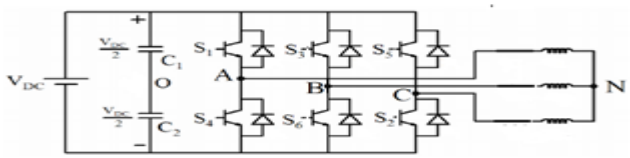

Figure 3: Inverter Block Diagram (Phuong, 2012**)**

Figure 4 below shown the eight switching configuration of a three-phase inverter.

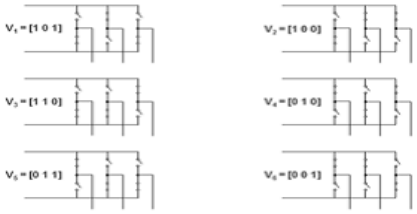

Figure 4: Inverter Legs States [23].

The line-to-line voltage vector $[V_{a\text{-}b}, V_{b\text{-}c}, V_{c\text{-}a}]$ is given as follows [21].

$$\begin{bmatrix} V_{a\text{-}b} \\ V_{b\text{-}c} \\ V_{c\text{-}a} \end{bmatrix} = V_{d\text{-}c} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad (2)$$

Also, the phase voltage vector $[V_{a\text{-}n}, V_{b\text{-}n}, V_{c\text{-}n}]$ can be expressed as follows [21].

$$\begin{bmatrix} V_{a\text{-}n} \\ V_{b\text{-}n} \\ V_{c\text{-}n} \end{bmatrix} = \frac{V_{d\text{-}c}}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad (3)$$

III SYSTEM DESIGN AND MODELLING

A. Choosing of DC Voltage Value

The minimum value of Vdc was calculated using equation 4 [20].

$$V_{d\text{-}c} \geq \sqrt{3}Vpmax \quad (4)$$

Vpmax = 400V

The required minimum of V_{dc} was calculated to be 693V. Therefore, 700V was chosen.

B. Choosing of Coupling Inductor Value

The minimum value of interfacing inductor was calculated using equation 5

$$Lc \geq \frac{V_{d\text{-}c}}{12fwI_{cmax}} \quad (5)$$

The converter maximum ripple current = 10A
Vdc = 693V (for modulation index = 1.7)
Switching frequency = 20 KHz.
The minimum value of L_c was calculated to be 2.88mH. Therefore, 3mH was chosen.

C. Choosing of DC Capacitor Value

The minimum value of DC capacitor was calculated using equation 6

$$c_{d\text{-}c} = \frac{S.f.T}{2kV_{d\text{-}c}^2} \quad (6)$$

The allowable compensator power transfer, S is 20kVA
Number of cycle, f = 0.5 (i.e half cycle)
Period, T for one complete cycle is 0.02S
Change in Vdc of 10% (i.e. k = 0.1)

Vdc = 693V (for modulation index = 1.7)
The minimum capacity of Cdc was calculated to be 2082µF. Therefore, 3000µF was chosen.

D. Shunt Active Power Filter modeling in d-q

The SRF method is implemented by transforming the three-phase source V_a, V_b and V_c and load current i_a , i_b , and i_c into the three-phase (d-q-0) synchronous reference frame in dc quantities as expressed as follows [15].

$$L_c \frac{di_{cd}}{dt} = V_{cd} - V_{id} - R_c i_{cd} - L_c \omega i_{cq} \quad (7)$$

$$L_c \frac{di_{cq}}{dt} = V_{cq} - V_{iq} - R_c i_{cq} + L_c \omega i_{cd} \quad (8)$$

E. Design of Space Vector Pulse Width Modulation (SVPWM)

Space vector pulse width modulation can be implemented by the following steps [16]

(i) Calculation of U_d, U_q, U_r and angle θ

(ii) Calculation of Time Duration T_{d0}, T_{d1} and T_{d2}

(iii) Transistors Switching Time Calculation

F. Calculation of U_d, U_q, U_r and Angle θ

Calculation of U_d, U_q, U_r and angle θ is carried out with the following equations as follow [16].

Direct voltage equation and quadrature voltage equation can be written as follows:

$$U_d = U_{a-n} - U_{b-n}\cos 60 - U_{c-n}\cos 60 \quad (9)$$

$$U_q = 0 + U_{b-n}\cos 30 - U_{c-n}\cos 30 \quad (10)$$

The reference voltage equation and alpha angle are writing as follows:

$$|U_r| = \sqrt{U_\alpha^2 + U_\beta^2} \quad (11)$$

$$\theta = \tan^{-1}\left(\frac{U_\alpha}{U_\beta}\right) \quad (12)$$

Where,

θ is the angle between reference voltage and alpha voltage

G. Calculation of Time Duration T_{d0}, T_{d1} and T_{d2}

The time of switching T_{d0}, T_{d1} and T_{d2} at any sector can also be achieved with the following equations as follow [17][18].

$$T_{d1} = \frac{\sqrt{3} T_d |\overline{U}_r|}{V_{d-c}} \left(\sin\frac{x}{3}\pi\cos\theta - \cos\frac{x}{3}\pi\sin\theta\right) \quad (13)$$

$$T_{d2} = \frac{\sqrt{3} T_d |\overline{U}_r|}{V_{d-c}} \left(\sin\left(\theta - \frac{x-1}{3}\pi\right)\right) \quad (14)$$

$$T_{d0} = T_d - T_{d1} - T_{d2} \quad (15)$$

Where,

T_d is the total time duration, T_{d1} and T_{d2} are boundary sector switching time duration, T_{d0} is the time duration at zero sector and x = (1 to 6).

H. Transistors Switching Time Calculation

Transistors switching time at each sector is computed in Table 2 [22][25].

Table 2: Transistors Switching Time Calculation at Each Sector

Sector	Switches S1, S3, S5	Switches S4, S6, S2
1	$S1 = T_{d1} + T_{d2} + T_{d0}/2$ $S3 = T_{d2} + T_d/2$ $S5 = T_{d0}/2$	$S4 = T_{d0}/2$ $S6 = T_{d1} + T_{d0}/2$ $S1 = T_{d1} + T_{d2} + T_{d0}/2$
2	$S1 = T_{d1} + T_{d0}/2$ $S3 = T_{d1} + T_{d2} + T_{d0}/2$ $S5 = T_{d0}/2$	$S4 = T_{d2} + T_d/2$ $S6 = T_{d0}/2$ $S1 = T_{d1} + T_{d2} + T_{d0}/2$
3	$S1 = T_{d0}/2$ $S3 = T_{d1} + T_{d2} + T_{d0}/2$ $S5 = T_{d2} + T_d/2$	$S4 = T_{d1} + T_{d2} + T_{d0}/2$ $S6 = T_{d0}/2$ $S1 = T_{d1} + T_{d0}/2$
4	$S1 = T_{d0}/2$ $S3 = T_{d1} + T_{d0}/2$ $S5 = T_{d1} + T_{d2} + T_{d0}/2$	$S4 = T_{d1} + T_{d2} + T_{d0}/2$ $S6 = T_{d2} + T_d/2$ $S1 = T_{d0}/2$
5	$S1 = T_{d2} + T_d/2$ $S3 = T_{d0}/2$ $S5 = T_{d1} + T_{d2} + T_{d0}/2$	$S4 = T_{d1} + T_{d0}/2$ $S6 = T_{d1} + T_{d2} + T_{d0}/2$ $S1 = T_{d0}/2$
6	$S1 = T_{d2} + T_d/2$ $S3 = T_{d0}/2$ $S5 = T_{d1} + T_{d0}/2$	$S4 = T_{d0}/2$ $S6 = T_{d1} + T_{d2} + T_{d0}/2$ $S1 = T_{d2} + T_d/2$

III. RESULTS AND DISCUSSION

A. Waveform of the Developed Model with Balanced Input Voltage

Figure 8 shows the Waveforms prior to compensation and Figure 9 shows the waveforms after compensation with the developed model. The waveforms of the developed model show that, the source current (Is) is now an ideal sinusoidal and rotates with the same angle with input voltage (Vs) when compared with the waveform in Figure 8.

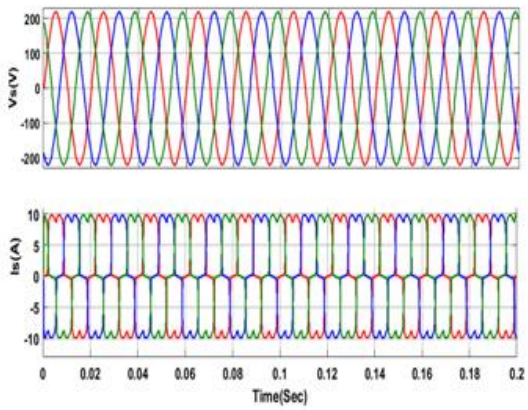

Figure 8: Waveforms prior to compensation

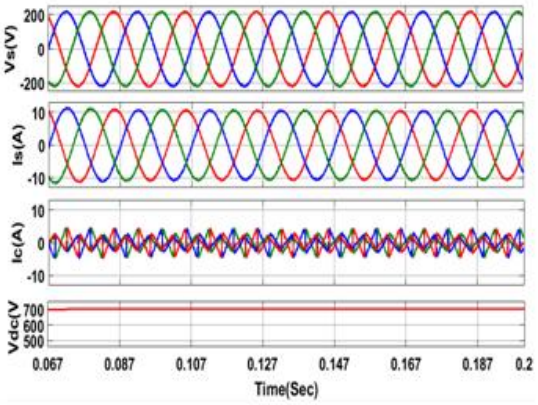

Figure 9: Waveforms after compensation with developed SVPWM

B. Analysis of Developed Model with Balanced Input Voltage

Figure 10 shows the Fast Fourier Transformation (FFT) analysis of source current prior to compensation and Figure 11 shows the FFT analysis of source current after compensation. The developed model achieved a significant 0.91% reduction in THD when compared to 25.60% prior to compensation and better performance than 1.13% of SPWM in Figure 12.

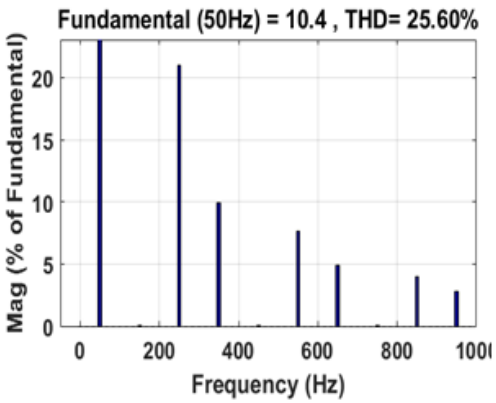

Figure 10: FFT Analysis prior to Compensation

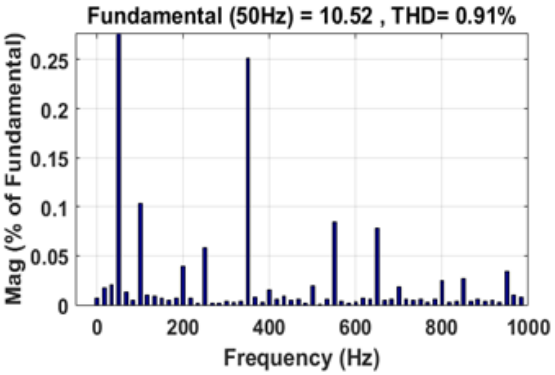

Figure 11: FFT Analysis with developed SVPWM

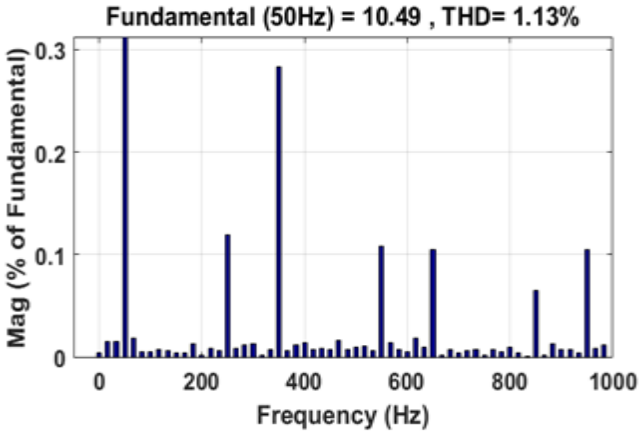

Figure 12: FFT Analysis with SPWM

C. WAVEFORM OF THE DEVELOPED MODEL WITH UNBALANCED INPUT VOLTAGE VOLTAGE

The developed model was tested with unbalanced input voltage of $V_A = 200V$, $V_B = 210V$, $V_C = 220V$.

Figure 13 shows the Waveforms prior to compensation and Figure 14 shows the waveforms after compensation with the developed model. The waveforms of the developed model show that, the source current (Is) is now an ideal sinusoidal and rotates with the same angle with input voltage (Vs) when compared with the waveform in Figure 13.

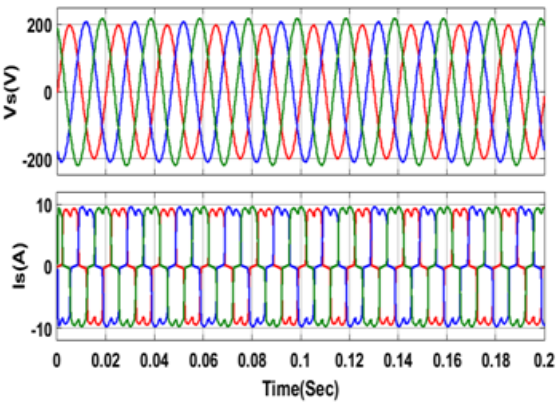

Figure 13: Waveforms prior to compensation

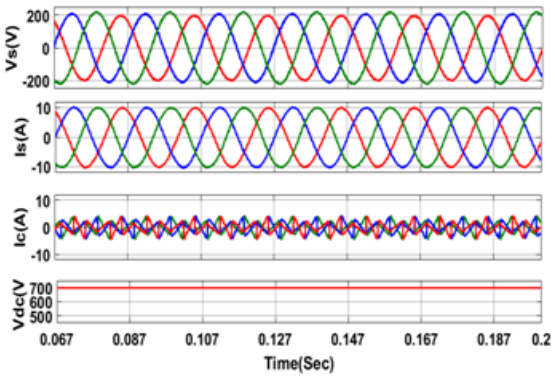

Figure14: Waveforms after compensation with developed SVPWM

D. FFT ANALYSIS OF DEVELOPED MODEL WITH UNBALANCED INPUT VOLTAGE

Figure 15 shows the Fast Fourier Transformation (FFT) analysis of source current prior to compensation and Figure 16 shows the FFT analysis of load current after compensation. The developed model achieved a significant 1.74% reduction in THD when compared to 26.68% prior to compensation and better performance than 1.85% of SPWM in Figure 17

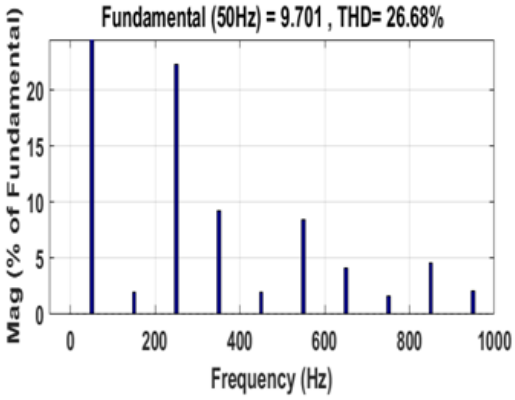

Figure 15: FFT Analysis prior to Compensation

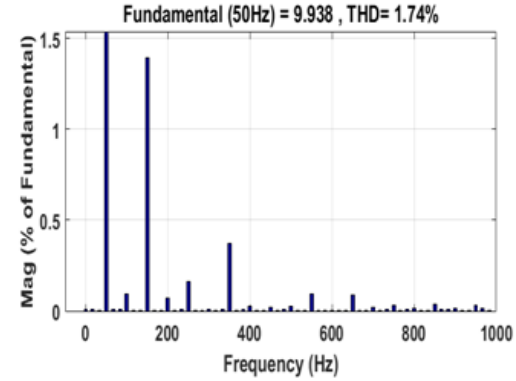

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Figure 16: FFT Analysis with developed SVPWM

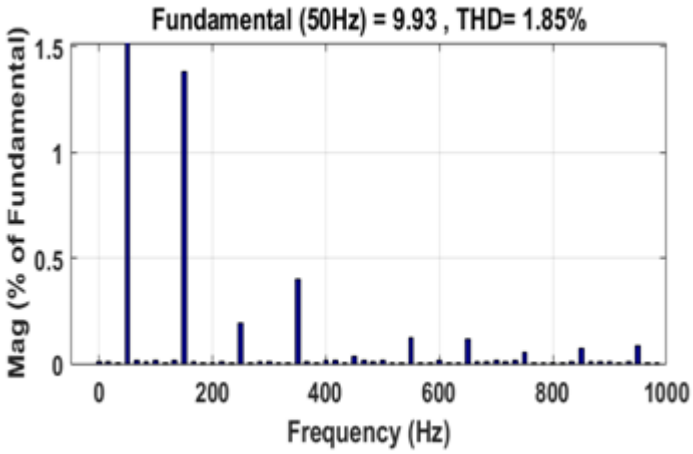

Figure 17: FFT Analysis after Compensation with SPWM

TABLE 2: RESULTS SUMMARY

Voltage	Control Strategy	THD without SAPF	THDs with SAPF	
			SVPWM	SPWM
Balanced	SRF	25.60	0.91	1.13
Unbalanced	SRF	26.68	1.74	1.85

IV. CONCLUSION

The developed model was tested for both balanced and unbalanced sinusoidal input voltage. FFT analysis shows that harmonic has been reduction from 25.60 % to 0.91 % (THD) for balanced input voltage and 26.68% to 1.74% for unbalanced input voltage using SVPWM. SPWM also reduced harmonic from 25.60% to 1.13% under balanced input voltage and 26.68% to 1.85% under unbalanced input voltage. The results show that the developed model performed better than SPWM.

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