Advanced Modeling and Design of Memristor Emulators: A Multilevel Approach

Arvi Naranjo-Calderón[1], Arturo Sarmiento-Reyes[1] & Wilfrido Calleja-Arriaga[1]
[1]*National Institute of Astrophysics, Optics and Electronics, Puebla, México*

ABSTRACT : *This article introduces two different approach models for afloating-type memristor emulators, using active building-blocks andtransistor-level simulations. The proposed emulator includes thefollowing components: CCTA, CCII, capacitor, and resistors, which allowfor a stable operation at frequencies up to 40 MHz. The first modelfocuses on the system-level emulator, and after some detailed analysisand design, the system shows good funciomality; the second model presentsa design parameter-based model which contain more detailed MOSemulation. Implementation of the emulator follows using the TSMC's 180nm CMOS technology. The circuit and model exhibit inherent memristorcharacteristics, including configurations in both decremental andincremental modes. Finally, validation and checking functionality of theproposed circuit, follow making simulations using Cadence software andTSMC's 180 nm technology, under typical operating conditions with asupply voltage of ±1.5 V.*

I. INTRODUCTION

The discovery of the memristor, first theorized by Leon Chua in 1971[1], marked a milestone in the history of electronics and circuit theory. Chua demonstrated that the memristor was the fourth fundamental passive circuit element, alongside the resistor, capacitor, and inductor, thus completing the theoretical framework of electronics with a component whose resistance depends on the history of the current passing through it. However, it was not until 2008 that the team at HP Labs[2], led by Stanley Williams, achieved the first practical demonstration of a memristor. This discovery not only completed the basic theory of circuits but also paved the way for revolutionary applications in non-volatile memory[3], neuromorphic computing[4], [5], [6], and artificial intelligence[7], given the memristor's unique ability to emulate synaptic plasticity[8].

Despite their promising future, the commercial-scale manufacturing of memristors faces significant obstacles, driving the development of CMOS memristor emulators[9], [10], [11], [12], [13], [14], [15]. These emulators are crucial for research and development, allowing for the exploration of memristor properties without the complexities of their physical fabrication. They are notable for their integration with conventional technology and for opening possibilities in advanced electronic systems.

The inherent challenges in the manufacturing and characterization of physical memristors have driven the development of memristor emulators as key tools for research and practical application. This work advances the design of these emulators through a multi-level approach that integrates both system-level modeling and design parameter-specific modeling, culminating in transistor-level design. Through these approaches, the aim is not only to better understand the unique properties of memristor emulators but also to improve the accuracy in simulating their behavior, thereby facilitating the exploration of their potential applications. This multi-level method allows for more effective addressing of the challenges in memristor emulation, significantly contributing to the precision and applicability of emulator designs.

This article begins with a review of the building blocks and their properties, as developed in Section II, setting the foundation for subsequent modeling and design. Section III details the development of the memristor emulator model at the system level, along with its preliminary results. Section IV presents the model based on design parameters, highlighting how this approach contributes to the accuracy and effectiveness of the final emulator design. In Section V, the design of the memristor emulator at the transistor level is described,

including simulation results and comparisons with existing emulators. Finally, Section VI summarizes the key conclusions of this study.

II. BUILDING BLOCKS AND THEIR PROPERTIES

The CCTA (Current Conveyor Transconductance Amplifier), proposed by Prokop et al. in 2005[16], is an electronic device designed to process current signals, unlike traditional voltage amplifiers that handle voltage signals. This device benefits from its capacity for applications where current processing is essential.

Comprising a second-generation current conveyor (CCII)[17] and a dual-output operational transconductance amplifier (OTA), the CCTA facilitates the efficient conversion of input currents into high-impedance outputs and the modulation of the output voltage into currents with varied gains. The synergy between the CCII and the OTA allows for precise manipulation of signals, highlighting its utility in advanced electronic circuits, as illustrated in Fig. 1
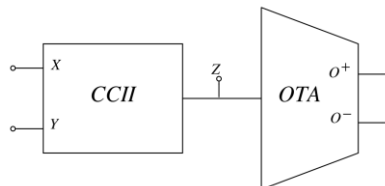

Fig.1: Structure of a CCTA.

The OTA is a device used to amplify the output voltage from the CCII and convert it into output currents with different gains. The OTA has two outputs, one that produces an output current proportional to the output voltage, and another that produces an inversely proportional output current to the output voltage. This allows the CCTA to be used for amplifying, filtering, and processing current signals in various ways; its symbol is shown in Fig. 2(a).

The CCII is a device used to transfer current from one point to another in a circuit. When a voltage is applied to the CCII's input, an output current is generated that is proportional to the input current. The CCII also has the property that the voltage at input X is equal to the voltage at input Y, making it useful in applications where a stable voltage reference is needed. The circuit symbol is shown in Fig. 2(b). The port relationships of the CCTA and CCII blocks are expressed as:

$$\begin{aligned}
I_Y &= 0, \\
V_X &= V_Y, \\
I_Z &= I_X, \\
I_o &= \pm g_m V_Z
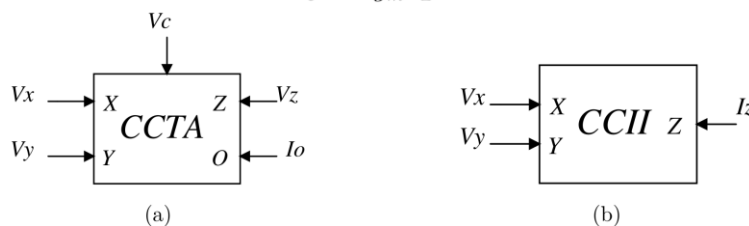\end{aligned}$$

(1)

(a)   (b)
Fig. 2: (a) Symbols (a) CCTA and (b) CCII.

Where g_m from equation 1 is the transconductance of the OTA given as:

$$g_m = \frac{k}{\sqrt{2}}(V_c - V_{ss} - 2V_{th})\sqrt{\left(\frac{W}{L}\right)}$$

(2)

Here, k is a constant that depends on the technology and is expressed as:

$$k = \mu C_{ox}\frac{W}{L}$$

(3)

$\mu_n, \frac{W}{L}$ y C_{ox} are the carrier mobility, aspect ratio, and oxide capacitance, respectively, while V_{th} represents the threshold voltage.

III. DEVELOPMENT OF THE MEMRISTOR EMULATOR MODEL AT THE SYSTEM LEVEL

The model is based on the circuit shown in Fig. 3, which uses analog active building blocks and is designed to emulate the behavior of a memristor. This model facilitates the research and study of the properties of the memristor emulator, allowing for the simulation of key properties, including the nonlinear dependence between voltage and current.

The model is constructed through a step-by-step analysis of the interactions between the circuit components and their electrical relationships. The input current I_{in} is initially defined in terms of the voltage at node A and the resistance R_1. This relationship is crucial for linking the input signal with the internal behavior of the circuit. Given the relationship $V_x = V_y$ in the CCII and considering that $I_y = 0$, it can be deduced that the voltage at node X_1 is primarily defined by the resistance R_1 and the input source, establishing a direct connection between the input signal and the internal state of the circuit.

Furthermore, the current flowing through the CCII, I_z, is equal to I_x, implying that the same input current flows through the terminals Z_1, Z_2, and Z_3 of the CCII. This property is essential for modeling the flow of current in the circuit.
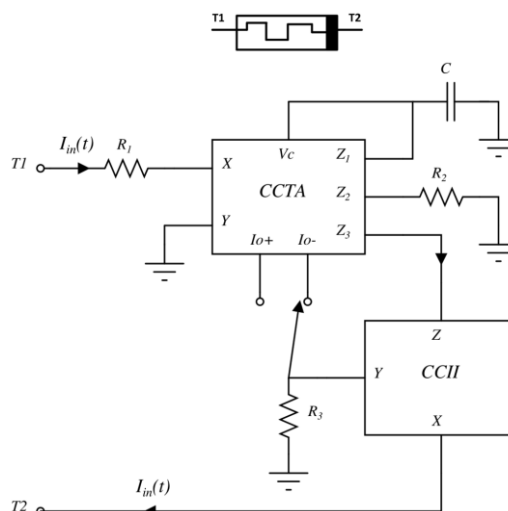

Fig. 3: Memristor emulator circuit.

Analysis of the OTA and Its Contribution to the Model

The OTA plays a crucial role in the circuit, with its output current I_o defined by the relationship $\pm g_m \cdot V_z$. This relationship introduces a nonlinear dependency in the model, an essential characteristic of memristors. The term V_z in the OTA is defined as the voltage difference across its inputs, thereby linking the behavior of the OTA to variations in the input voltage. The transconductance g_m, a key parameter of the OTA, is directly related to the input current and the value of the capacitor, according to the expression $g_m = \beta \left(\frac{I_{in}}{sC} - V_\phi \right)$. This relationship is crucial for establishing how the input current affects the output current of the OTA, and therefore, the overall dynamics of the circuit.

System Differential Equation

Integrating all these relationships and analyses, the differential equation that describes the behavior of the system is formulated. This equation reflects not only the interactions among the components but also how the sinusoidal input signal V_{in} affects the circuit dynamics ($V_{in} = A_p \sin(\omega t)$). The differential equation is expressed as:

$$\frac{dx}{dt} = \beta \left(\frac{x}{C} - V_\phi \right) \cdot \left(\frac{R_2 \cdot V_{in}}{R_1 - R_3} \right) \tag{4}$$

This equation captures the essence of the memristor's behavior, modeling how the output current $x(t)$ evolves over time in response to the input signal.

Solution of the Differential Equation

Following the solution of the differential equation, equation 5 provides the fully symbolic model of the emulator.

$$x(t) = \frac{A_p \sin(\omega t)\, R_2 V_\phi \beta\, \mathrm{e}^{\frac{\beta A_p R_2 \cos(\omega t)}{(R_1 + R_3)\omega C}}}{(R_1 + R_3)\, \mathrm{e}^{\frac{\beta A_p R_2}{(R_1 + R_3)\omega C}}} \tag{5}$$

This solution reveals the emulator's response to the sinusoidal input, highlighting the nonlinear and time-dependent characteristics of the memristor. The memristance model is expressed in equation 6.

$$M(t) = \frac{(R_1 + R_3)\, \mathrm{e}^{-\frac{\beta A_p R_2 (\cos(\omega t) - 1)}{(R_1 + R_3)\omega C}}}{R_2 \beta V_\phi} \tag{6}$$

3.1 Model Characterization and Parameter Analysis

The values corresponding to the model parameters are shown in Table 1. All characterization will be done at a frequency of 40 MHz.

Table 1: Model parameter.

Parameter	Value
$R1$	$1.2\ k\Omega$
$R2$	$2.9\ k\Omega$
$R3$	$0.6\ k\Omega$
C	$1.2\ pF$
V_ϕ	1.5
β	$648\ \mu$

R_1 **Analysis:** Figs. 4(a) and 4(b) demonstrate the response of the memristor emulator to varying the resistance R_1. The I-V curves display a sequence of hysteresis loops that decrease as R_1 is increased, highlighting the emulator's sensitivity to resistance in the current path. An increase in R_1 results in a smaller hysteresis area. Correspondingly, the memristance, illustrated in the M-I curves (Fig. 4(b)), exhibits higher and broader peaks when R_1 is lower. The correlation between the I-V and M-I characteristics underscores how resistance controls the amplitude and memristance of the emulator.

C **Analysis:** The influence of capacitance on the behavior of the memristor emulator is shown in the I-V curves of Fig. 4(c) for different capacitance values, ranging from 1 pF to 5 pF. These indicate that a lower capacitance leads to wider hysteresis loops, yielding higher memristance values. This behavior is reinforced by the M-I curves of Fig. 4(d), where memristance increases and peaks shift towards higher current values with decreasing capacitances. This phenomenon illustrates the emulator's ability to modify its response based on charge storage, which is a key attribute for emulating memristive properties.

β **Analysis:** Fig. 4(e) shows the current-voltage characteristics of the memristor emulator as the β parameter is varied. An increase in this parameter denotes a greater response of the emulator to the applied stimulus and suggests a stronger dependence on the device's previous state, which is consistent with a greater effect of the control signal V_c on the memristor's memristance. The corresponding M-I curves of Fig. 4(f) show that memristance reaches higher maximum values for increased values of β. It is interesting to note that as β decreases, the ranges of minimum and maximum memristance values shift to lower ranges, meaning that increasing this parameter causes the current to increase but, on the other hand, memristance features are diminished.

By correlating the observed behaviors for R_1, C, and β with the emulator model, a complex and multifaceted interaction underlying the memristive behavior is evidenced. The resistance R_1 directly affects the amplitude of the input current, C introduces an effect directly on the area of the hysteresis loop making it larger if C decreases, and β modulates the emulator's reactivity to input signals. Each parameter influences the dynamic signature of the emulator's response, allowing for a wide range of adjustments in the memristive properties of the emulator. This versatility highlights the emulator's potential to simulate various synaptic functions in neuromorphic circuits, as well as for applications in non-volatile data storage systems.
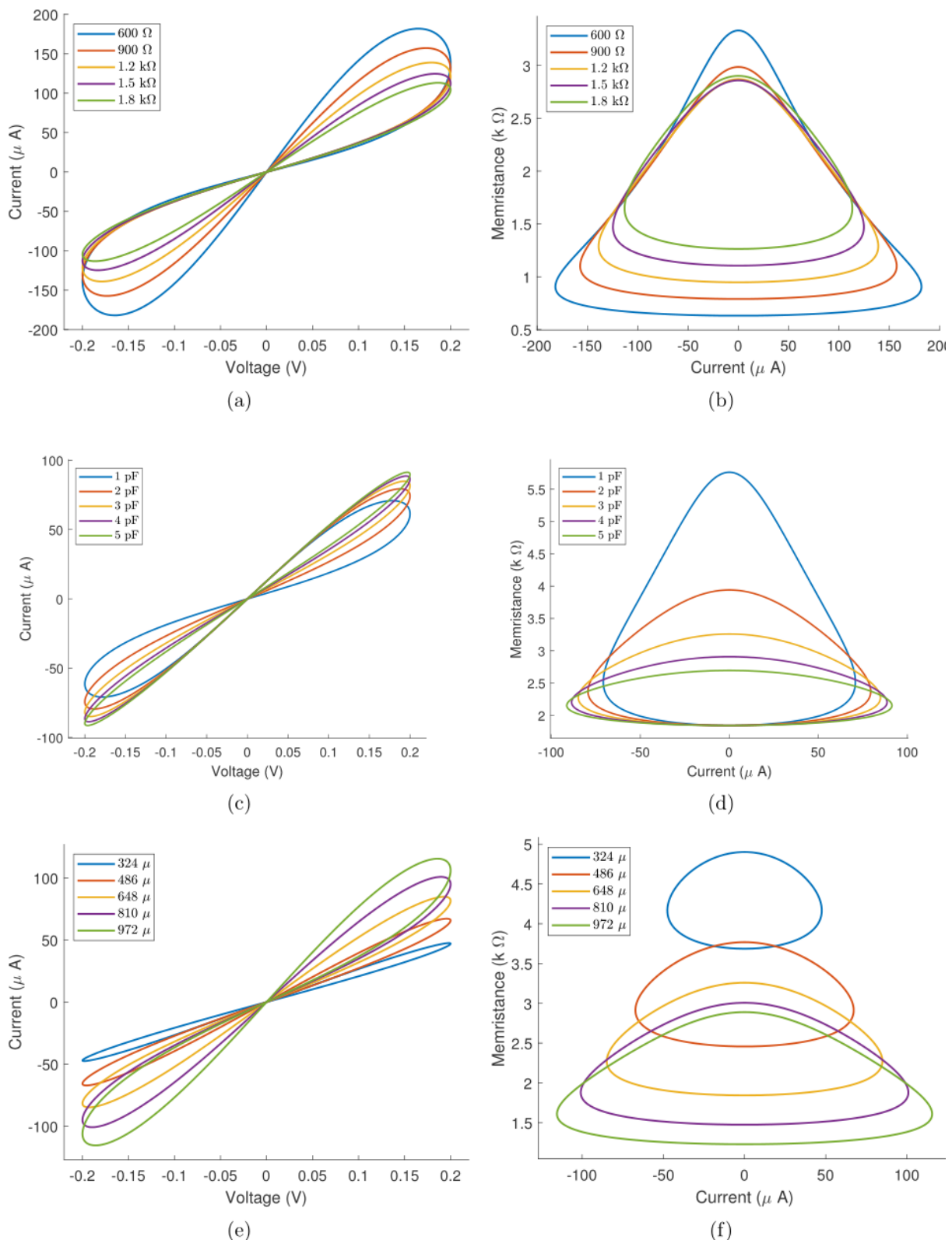
Fig.4: Characterization for different values of R_1, (a) hysteresis loops, (b) current-memristance curve, Capacitance (c) hysteresis loops, (d) current-memristance curve, β (e) hysteresis loops, (f) current-memristance curve.

3.2 Hysteresis Loop Area

In this section, we will explore how the area of the hysteresis loop in a memristor, a key indicator of its dynamic behavior, is influenced by various model parameters. This analysis is crucial for understanding how memristors respond to different operating conditions and how these behaviors can be modeled and applied in circuit design.

The area of the hysteresis loop of a memristor is an important parameter that can provide valuable information about the behavior of the memristor. The hysteresis loop is a graphical representation of the relationship between voltage and current.

To calculate the area of the hysteresis loop, the hysteresis curve is integrated on the current versus voltage graph. The general formula for calculating the area of the hysteresis loop is expressed in the following equation:

$$A = \oint_0^{\frac{T}{2}} V \cdot dI$$

(7)

Where V represents the voltage and I represents the current through the device. The integral is taken over the range of 0 to $\frac{T}{2}$, which corresponds to the area of one of the lobes of the hysteresis loop.

Once the nominal values of the parameters in the memristor model are known, a detailed analysis can be conducted to determine how each of these parameters affects the area of the hysteresis loop. This analysis is important because it allows us to understand how changes in parameters can affect the hysteresis area. Additionally, this information can be useful for designing circuits that make the most of the memristor's properties in terms of a larger area in the hysteresis loop. Equation 8 shows the symbolic expression of the hysteresis lobe area.

$$A = \frac{\left(\left(\cos^2\left(\frac{\omega T}{2}\right)\right)R_2^2\beta^2 - R_2^2\beta^2\right)e^{\frac{R_2 A_p \beta\left(\cos\left(\frac{\omega T}{2}\right)-1\right)}{(R_1+R_3)\omega C}} V_\phi A_p^2}{(R_1+R_3)R_2\beta}$$

$$+ \frac{\left(-CR_2\beta\omega(R_1+R_3)\cos\left(\frac{\omega T}{2}\right)e^{\frac{R_2 A_p \beta\left(\cos\left(\frac{\omega T}{2}\right)-1\right)}{(R_1+R_3)\omega C}} + (R_1+R_3)\omega CR_2\beta\right)V_\phi A_p}{(R_1+R_3)R_2\beta}$$

$$+ \frac{\left((R_1+R_3)^2\omega^2C^2 e^{\frac{R_2 A_p \beta\left(\cos\left(\frac{\omega T}{2}\right)-1\right)}{(R_1+R_3)\omega C}} - (R_1+R_3)^2\omega^2C^2\right)V_\phi}{(R_1+R_3)R_2\beta}$$

(8)

Fig. 5(a) illustrates the relationship between the hysteresis area of the memristor emulator and the value of the resistance R_1. The curve shows a monotonic decrease in the area as R_1 is increased from 600 Ω to 1800 Ω. The decrease in the area with the increase of R_1 suggests that a higher resistance limits the current flowing through the memristor for a given applied voltage, thus reducing the amount of energy that can be stored and dissipated during each cycle. The area equation (equation 8) of the memristor emulator, which incorporates the resistance R_1 as part of an exponential term, supports this interpretation. Resistance R_1 appears in the denominator of this term, indicating that higher values of R_1 attenuate the exponential response and, therefore, decrease the variability of the hysteresis area.

Fig. 5(b) shows a decreasing relationship between the hysteresis area of the memristor emulator and the circuit's capacitance. It is observed that as the capacitance increases from 1.5 pF to 4.5 pF, the hysteresis loop area decreases linearly. With lower capacitances, the circuit's time constant is smaller, allowing for quicker changes in the circuit's response. This can make the circuit more sensitive to rapid variations in Vin, which could explain why the hysteresis loops become wider Fig. 5(e). However, the inverse relationship suggests that an increase in capacitance is influencing the memristor's response speed to voltage changes in a way that effectively reduces the energy dissipated in each cycle. This may be due to the current taking longer to reach its maximum value as capacitance increases, thus reducing the amplitude of the current signal in response to a specific voltage stimulus.

On the other hand, the exponential dependency in equation 8 shows how the input current varies with capacitance and input voltage. The key here is how the capacitance C influences the exponential term. With a lower capacitance, the effect of the exponential can increase, as decreasing C raises the value of the negative exponent, which can lead to greater variability in the I_{in} response for different V_{in} values.

Moreover, as shown in Fig. 5(c), a directly proportional relationship between the hysteresis area of the memristor emulator and the β parameter is observed. It is noted that as β increases, the area of the hysteresis loop also increases, indicating that β significantly influences the emulator's response. The positive slope of the graph reflects the sensitivity of the hysteresis area to changes in β, and can be interpreted as a higher efficiency in converting applied energy into energy stored and dissipated in the form of hysteresis. The trend observed in the graph provides valuable data for the design and optimization of memristor emulators. Adjusting β allows for control over the amount of hysteresis in the device.
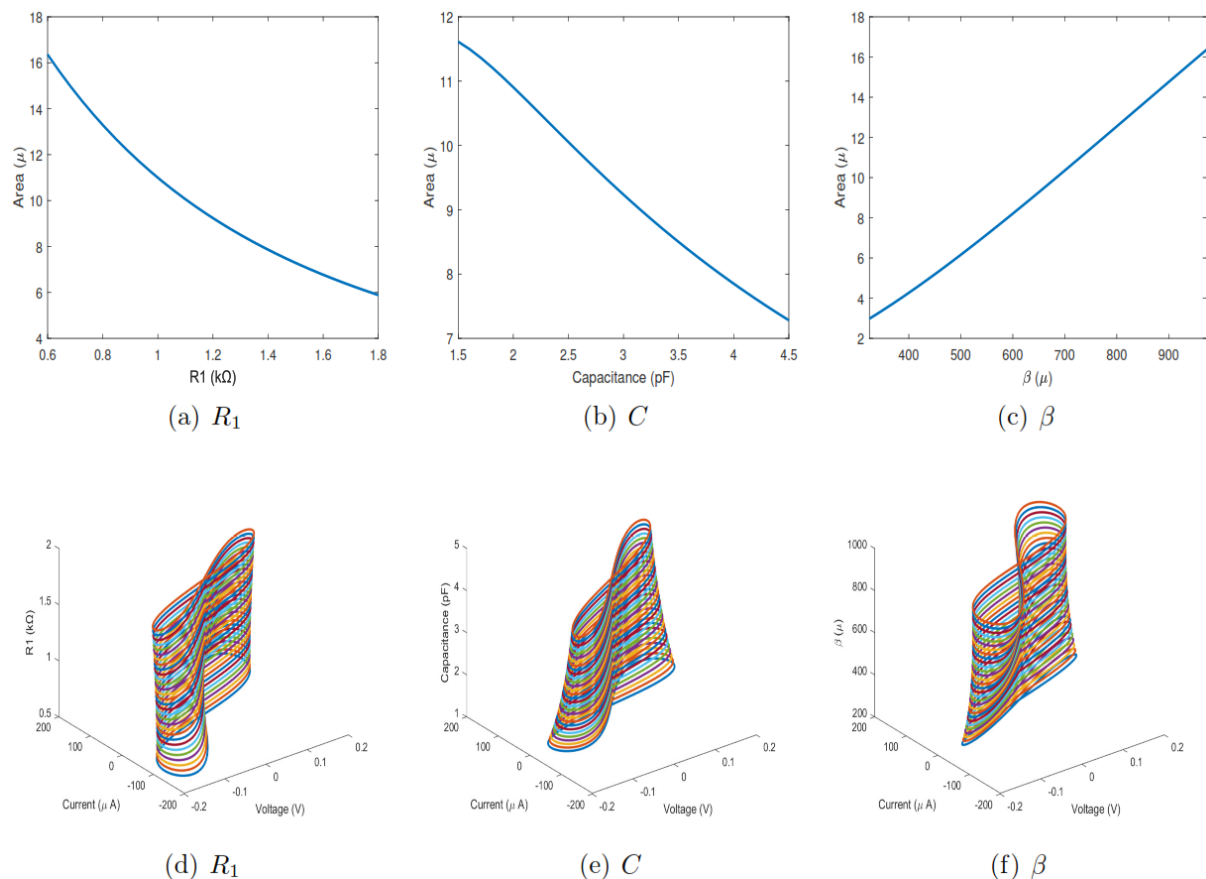

Fig.5: Area versus variation of the parameters.

The graph in Fig. 6 shows the relationship between the hysteresis area and the frequency of the stimulus signal, reflecting a key identity trait of memristors[18], [19]: as the frequency increases, the area of the hysteresis loop decreases, which is consistent with the theory that the response of the memristor is time dependent. At high frequencies, the charging time is insufficient for the memristor to significantly alter its resistance state, causing the hysteresis loop to shrink and tend towards a more linear response. This suggests that, at the limit of infinite frequency, the hysteresis could eventually disappear, reflecting the idealized behavior of a memristor whose response becomes purely resistive, without dependence on previous history, when operated at extremely high speeds.
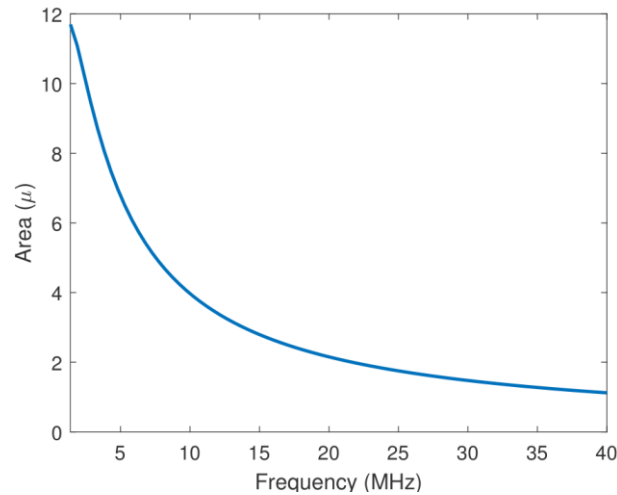
Fig.6: Area versus frequency.

3.3 Sensitivity Analysis

Sensitivity analysis focuses on determining how small variations in the parameters of the memristor significantly affect the area of the hysteresis loop. This understanding is vital for the precise design of memristors.

The sensitivity of a function with respect to a parameter is the measure of the variation experienced by the function when the value of the parameter changes. The sensitivity of a function A with respect to a parameter x can be calculated using the following formula:

$$S_x^H = \frac{x}{A} \cdot \frac{\partial A}{\partial x} = \frac{\partial lnA}{\partial lnx}$$

(9)

Where $\frac{\partial A}{\partial x}$ is the partial derivative of A with respect to x and $\frac{x}{A}$ is the ratio of the value of x to the value of A.

The analysis of the hysteresis area sensitivity graphs in relation to the parameters R_1, C, and β reveals critical aspects of the behavior of the memristor emulator under variations in these circuit components. In the graph of Fig. 7(a) corresponding to R_1, it is observed that the sensitivity of the hysteresis area decreases as R_1 increases, showing a downward curve. This indicates that increments in R_1 have an attenuating effect on the variability of the hysteresis area, suggesting that the higher the resistance, the lesser is the influence of R_1 on the memristor's ability to alter its state of maximum memristance in response to the stimulus signal as seen in Fig. 4(b).

The graph in Fig. 7(b) is sensitivity as a function of capacitance C, showing a decreasing trend, meaning that as the circuit's capacitance increases, the sensitivity of the hysteresis area decreases. This is interpreted as an increase in the memristor emulator's ability to store electrical charge without a significant alteration in its resistance state, resulting in a smaller hysteresis area and lower maximum memristance as shown in Fig. 4(f). Lastly, the sensitivity graph with respect to β (Fig. 7(c)) presents a linear negative slope, which reflects that, although the hysteresis area may be larger when β increases, the degree of this influence decreases the ranges of initial and maximum memristance as β is increased as can be seen in Fig. 4(d).

These sensitivity graphs are essential for understanding how each of these parameters affects the fundamental characteristics of the memristor and are crucial for the design and optimization of memristor emulators that can be finely adjusted for specific applications.
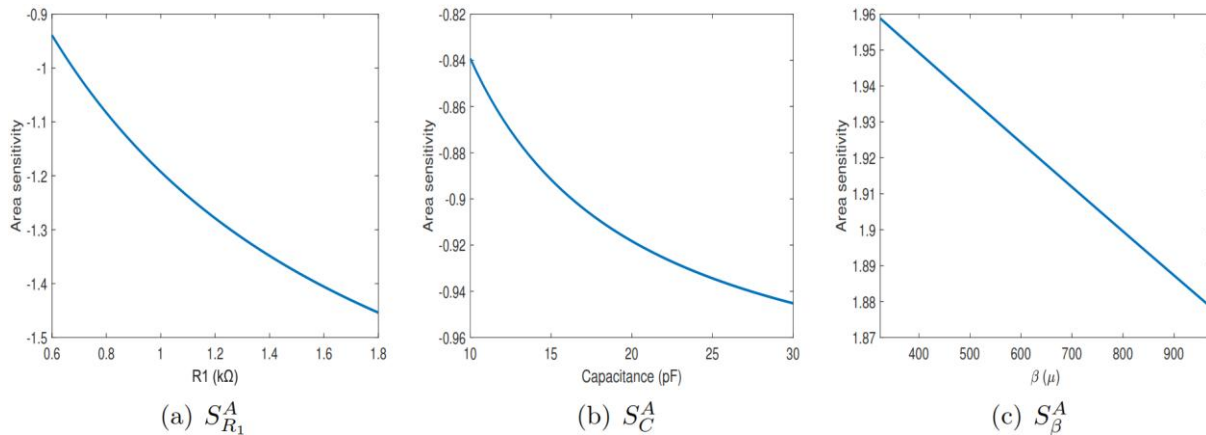
Fig. 7:Area sensitivity of the hysteresis lobe.

IV. MODEL BASED ON DESIGN PARAMETERS

In this section, we present the development of a detailed model that encapsulates the intrinsic behavior of the memristor emulator, leveraging small-signal parameters for high accuracy. This model is distinguished by its comprehensiveness and analytical depth, reflecting the complex interaction among the CMOS emulator components to faithfully replicate a memristor's characteristics. Given the complexity and the extensive number of parameters, the complete model is available through the attached link[20], providing access to its entire structure. There, both the complete model and a simplified model are presented. The simplification method of this model was based on the aspect ratio of the transistors comprising the emulator. The model was constructed based on small-signal transistor-level parameters, such as g_m and G_{ds}. This model preserves the fundamental characteristics of memristor emulators, such as nonlinearity. The relevance of this design parameter-based modeling lies in its ability to offer an accurate representation of the systems and phenomena studied. This approach not only allows for a better understanding of these systems but also enables more effective prediction of their behavior. Moreover, these models are essential for design optimization, allowing for testing different configurations. The parameter values were obtained from a preliminary design from which the operating points were derived. Before parameter extraction, it ensures that the emulator is within the expected range.

Characterizing the model is an essential process to understand how each parameter influences the overall behavior of the memristor emulator. This stage involves a detailed analysis of each parameter. This analysis provides a deep understanding of how each model component contributes to the global operation of the emulator, establishing a solid foundation for optimized design. Parameter analysis focuses on determining the contribution of each parameter to the emulator's behavior. Qualitative and quantitative analysis techniques are employed to evaluate how variations in each parameter affect the size and shape of the hysteresis loop, a key indicator of memristor behavior.

The key steps in parameter analysis include:

1. **Parameter Sweep**: A sweep is performed for each parameter, adjusting its value within a range that includes a reference value, a value 50% lower, and a value 50% higher than the reference.

2. **Hysteresis Loop Analysis**: For each parameter setting, the hysteresis loop in the current-voltage plane is generated and analyzed. This analysis allows observing how changes in parameters affect the key properties of the emulator.

3. **Identification of Critical Parameters**: Based on the analysis results, parameters that have a significant impact on the emulator's behavior are identified.

Fig. 8 shows the graphs of hysteresis loops with different values of g_m. As can be noted in the graph of Fig. 8(a), (b), and (f), variations in g_m do not impact the hysteresis loop as much, unlike in graphs (c), (d), and (e), where greater changes in the hysteresis loop are shown.

It is notable how, in some transistors, these sweeps cause significant changes in the hysteresis loop. It is important to highlight that similar analyses were carried out for all model parameters. This allowed identifying which transistors exert a greater influence on the output results of the emulator. This knowledge is crucial for the emulator redesign process, a topic that will be addressed in the following section.
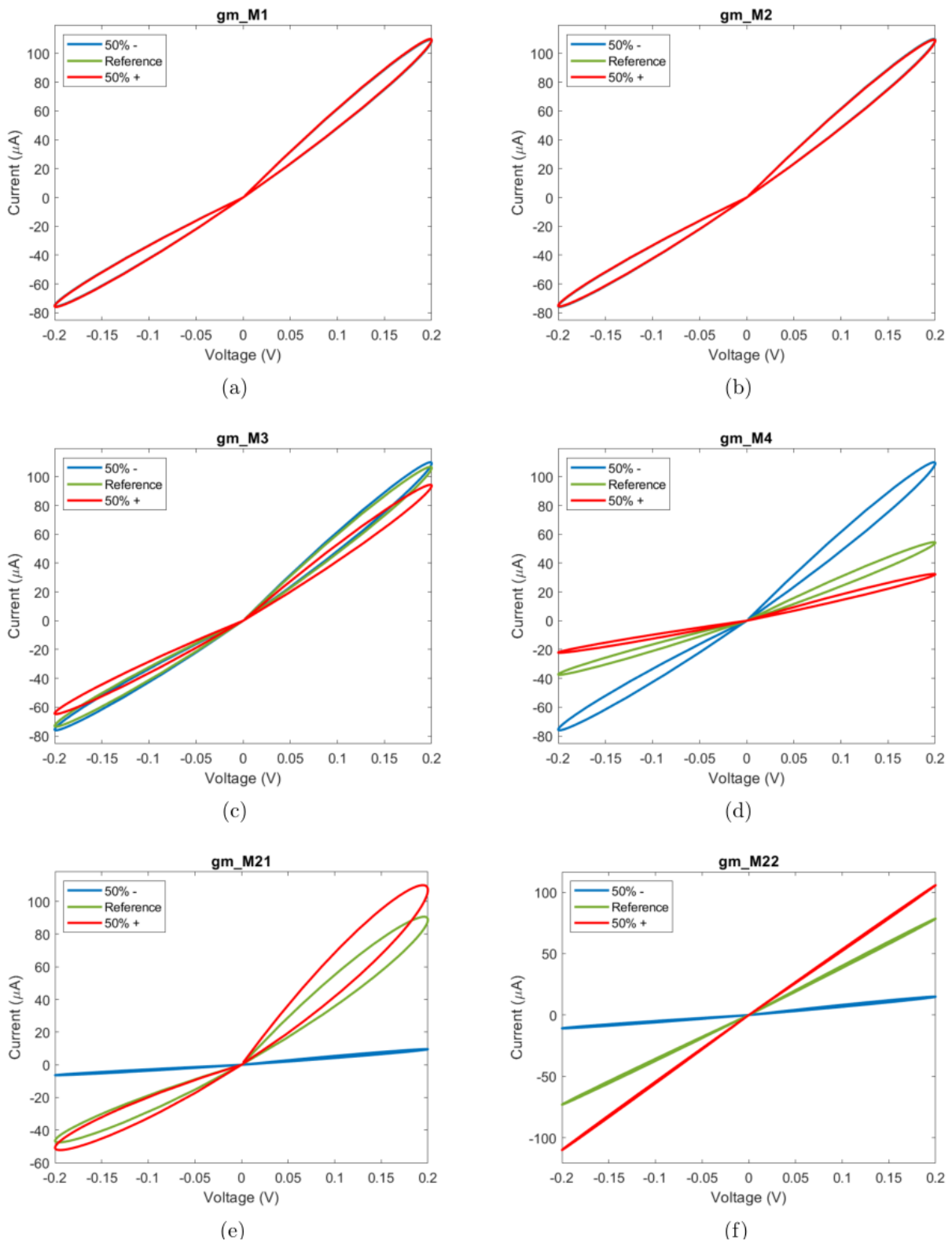
Fig. 8: Hysteresis loops of the model based on design parameters.

V. MOS EMULATOR

This section presents the CMOS design and performance of the floating type memristor emulator shown in Fig. 3. This emulator is capable of being configured in both incremental and decremental modes. The CMOS structure of the Current Conveyor Transconductance Amplifier and the Second-Generation Current Conveyor are shown in Fig. 9.

The accuracy in the transconductance of the CCTA is essential for achieving faithful emulation, being adjustable by modifying circuit parameters, such as the dimensions of the transistors and the bias voltage. On the other hand, the CCII is characterized by its ability to transfer current between its terminals, maintaining a high input impedance. In the CMOS schematic of the CCII, special emphasis is placed on the linearity of its response and its ability to operate over a wide range of frequencies. The simulation of this emulator was carried out in the Cadence Virtuoso design tool, using TSMC's $0.18 \ \mu m$ technology process.
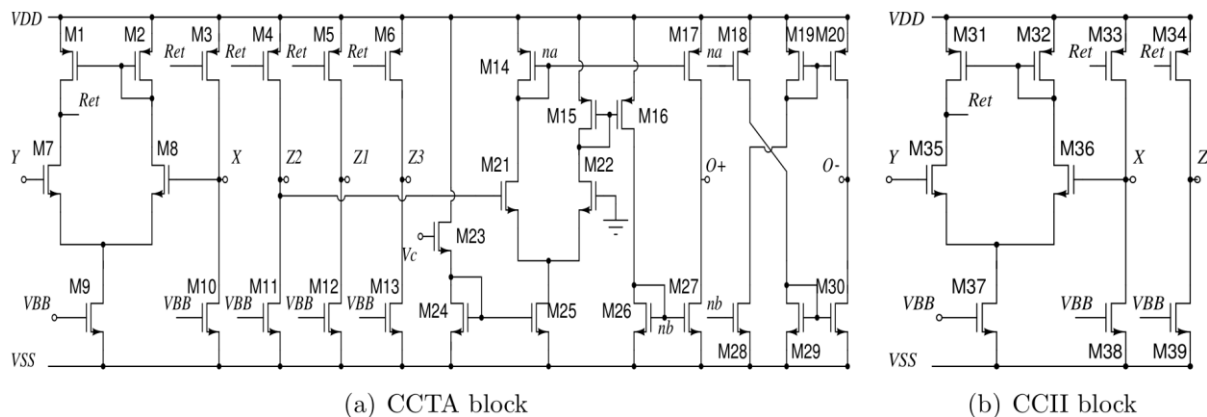

Fig. 9: CMOS implementation.

To ensure a thorough evaluation, simulations were conducted that clearly outline the current and voltage graphs as a function of time, revealing the internal dynamics of the emulator. Using a sinusoidal signal of $0.2V$ amplitude, with a power supply voltage of $\pm 1.5 \ V$ and a bias voltage of $V_{BB} = 400 \ mV$. The resistors R_1, R_2, and R_3 were set at values of $1.2 \ k\Omega$, $2.9 \ k\Omega$, and $0.6 \ k\Omega$ respectively, while a nominal capacitance value of 3 pF was established to capture the characteristic hysteresis phenomenon of memristors. The aspect ratio of the CMOS transistors, specified in Table 2, confirms their operation in the saturation region, crucial for the functioning of the emulator.

Table 2: Aspect ratio of MOS transistors.

NMOS	W(μm)/L(nm)
M7,M8, M35,M36	4.3/570
M21-M22	9.9/570
M25	4.8/570
M26-M30	2.4/570
M24	18.9/570
M23	33.9/570
M9, M37	8/570
M10-M13, M38-M39	9.6/570
PMOS	**W(μm)/L(nm)**
M1-M6, M31-M34	15.6/570
M14-M20	34.6/570

Fig. 10(a) displays the current and voltage curves against time, while Fig. 10(b) highlights the nonlinear nature of the emulator through hysteresis loops obtained at a frequency of 14 MHz with different capacitance values (2.9pF, 3pF, and 3.1pF). These hysteresis loops show the influence of the capacitor on the operation of the emulator; specifically, how an increase in capacitance leads to a reduction in the size and area of the hysteresis loop, aligning with the behaviors predicted by theoretical models and what is expected from an ideal memristor.
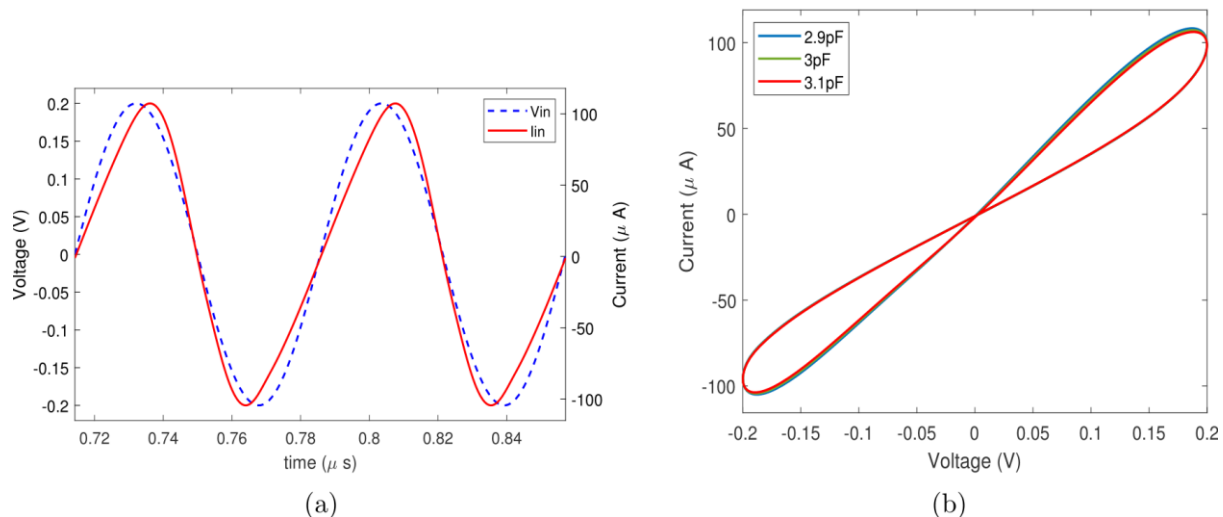
Fig. 10: (a) Transient analysis curves of the memristor emulator, (b) hysteresis loop at 14 MHz for different values of the capacitor.

Additionally, Fig. 11 shows the transient graphs of current and voltage, as well as the hysteresis loops for a frequency of 40 MHz. As can be seen in Fig. 11, there is a decrease in the area of the hysteresis loop as capacitance increases, with values of 1.15pF, 1.2pF, and 1.25pF.

The simulations have confirmed that the behavior of the emulator closely aligns with the theoretical predictions presented in Section III. A significant interdependence between frequency and capacitance ($\omega \cdot C$) is highlighted, which allows for maintaining a constant hysteresis area through fine adjustments in the parameters. For example, when increasing the frequency and wanting to preserve the area of the hysteresis loop, one can decrease the capacitance using a simple rule of three, thus maintaining the same loop area.
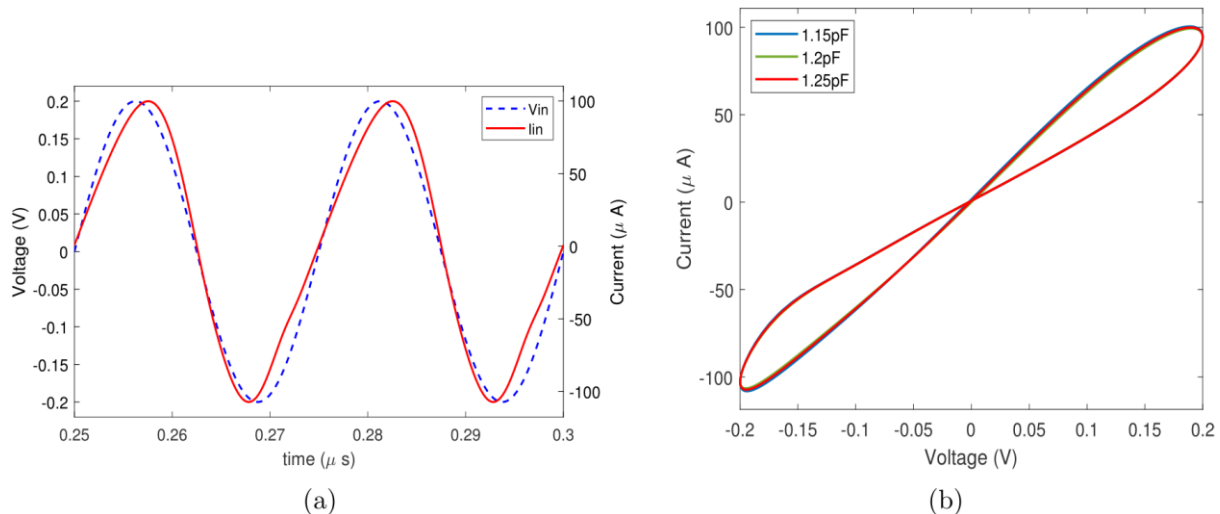

Fig. 11: (a) Transient analysis curves of the memristor emulator, (b) hysteresis loop at 40 MHz for different values of the capacitor.

VI. COMPARISON

Table 3 provides a comparison among various memristor emulators, highlighting the current work for its exceptional maximum operational frequency and its focus on the configuration of active blocks and passive elements. When observing the key differences, the emulator presented in this work surpasses its predecessors and contemporaries in several aspects:

1. **Maximum Operating Frequency**: With a maximum operating frequency of 40 MHz, the emulator from this study significantly outperforms the rest, indicating a superior ability to handle high-frequency signals, crucial for cutting-edge applications where speed and quick response are essential.

2. **Type of Connection**: The ability to operate in a floating (F) configuration makes it versatile and more suitable for a variety of circuit topologies, compared to those limited to ground-connected (G) configurations.

3. **Mode of Operation**: The ability to function in both incremental and decremental modes offers operational flexibility that makes it suitable for a wide range of applications, like several of the other designs.

4. **Compared to the work** [11], which uses 6 resistors, 2 capacitors, 1 MOSFET, and 2 operational amplifiers to develop the CVR, a greater complexity in its implementation is evident.

Table 3: Comparison with other memristor emulators.

Ref	# Active blocks	# Pasive elements	Tecnology used	Floating or Grounded	Incremental/ Decremental	Max. op. freq.
[9]	1 CCII, 1 VDIBA	1 R, 1 C	180 nm	G	—	25 MHz
[10]	1 DO-OTA. 1 DVCC 2 MOS	1 C	180 nm TSMC	F	Both	1.5 MHz
[11]	1 CCII+, 1 VCR	1 C	130 nm TSMC	G	—	1 MHz
[12]	1 DVCC, 1 OTA	1 R, 1 C	180 nm	G	Both	8 MHz
[13]	1 CCII, 1 OTA	1 R, 1 C	180 nm	G	Both	26.3 MHz
[14]	1 DVCCTA	2 R, 1 C	180 nm TSMC	G	Both	12 MHz
[15]	1 VDGA	1 C	180 nm TSMC	Both	Both	1 MHz
[21]	1 CDTA, 1 OTA	1 C	180 nm TSMC	G	Both	2 MHz
[22]	1 MVDCC	1 C	180 nm	F	Both	1.5 MHz
[23]	1 CFDITA	1 C	180 nm	Both	Both	10 MHz
This work	1 CCTA, 1 CCII	3 R, 1 C	180 nm TSMC	F	Both	40 MHz

VII.CONCLUSION

The research and development presented in this work constitute a significant advancement in the modeling of memristor emulators. The fundamental contribution of this study is centered on two complementary memristor emulator models, the first model based on the interaction of the elements that make up the circuit, and on the other hand, the model based on small-signal design parameters and its implementation through a CMOS design.

Model 1, characterized by its system-level approach, establishes a solid foundation for understanding the overall dynamics and distinctive characteristics of memristive behavior. Through a series of simulations and analyses, including the characterization of area sensitivity and other key metrics, a deep understanding of the effects of circuit parameters on the overall performance of the emulator is achieved. The ability to adjust memristive behavior by varying specific parameters provides a valuable tool for the design and optimization of memristor emulators.

Model 2 delves further, incorporating a level of detail based on transistor-level design parameters. This model is distinctive for its richness in detail, accurately capturing the complex interaction of small-signal parameters in a CMOS environment. This model's ability to predict the emulator's behavior across a broader range of operating conditions represents a significant advance, allowing for more precise and efficient emulation of memristors.

The implementation of a CMOS design for the memristor emulator stands out for its high maximum operational frequency of 40 MHz, demonstrating superior performance compared to existing emulators. This design benefits from the use of active blocks such as CCTA and CCII, in conjunction with multiple passive elements, to offer precise and flexible emulation of memristor behavior.

The models proposed, and their CMOS design represent a significant advance in memristor emulation. The comprehensive approach that combines theoretical analysis, simulation, and practical implementation lays the groundwork for future research and applications of memristors. The developed models not only demonstrate a significant improvement in emulation fidelity but also offer a robust platform for exploring new configurations and operating principles in the growing area of reconfigurable electronic components.

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