

Improved Integrated Circuit Multi-Tester

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Abstract- Generally, testing is proving the functional correctness of a product. When applied to Integrated Circuits (IC), testing of ICs refers to a series of tasks carried out to check the functionality of ICs. This is of great significance due to the roles ICs play in modern electronics and complex systems. Although numerous IC testers exist, most available are either too expensive to own by the average learner (undergraduates and graduate Engineers) and also do not have functionality for testing basic ICs like 555 timer ICs, Op-Amp, CMOS and TTL circuits as a single integrated unit. This dissertation thus entails the designing and implementation of an improved Integrated Circuit multi-tester with focus on the educational and engineering environments. The aim of this dissertation was to implement an improved and low-cost Integrated Circuit multi-testing device for users to perform Integrated Circuit chip testing on the commonly used digital ICs like the very popular 555 timers, Operational Amplifiers (Op-amps), Complementary Metal Oxide (CMOS) and Transistor-Transistor Logic (TTL) circuits. The objectives are to do a thorough literature review on existing work on integrated circuit testing, to develop an Algorithm and an Operational Flowchart to be implemented in the embedded ESP32 microcontroller, to implement the proposed system on an existing hardware and to validate the system by performing comparative analysis with existing IC testers. The design methodology utilized was bottom-up approach in which the Improved IC Multi-Tester was broken into smaller independent units which was then assembled as a whole. Functional testing was employed on the completed work to verify the functionality of the device under test and results were obtained. From the test results, an average measured frequency of 1306.18Hz as compared to a design frequency of 1307.1Hz with an average frequency deviation of ($\pm 3.4\%$) percent for a good and working 555 timer IC. An average gain of 3.19 was actually measured against an expected gain of 3.3. The acceptable percentage deviation range from the designed gain of 3.3 is ($\pm 5\%$) percent or . The improved IC multi-tester was able to test 14-pins CMOS and TTL categories of ICs and also 8-pins 555 timer and Op-Amp ICs.

Index Terms—Integrated Circuits (IC), Multi-tester,

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I. Introduction

Since the introduction of Very-Large-Scale Integration (VLSI) devices in the early 1980s, the complexity and density of digital circuits continue to increase; a single chip today can consist of millions of transistors measuring in nanometers Lee *et al* [1]. As circuit size increases with steadily decreasing transistors dimension, referred to as feature size, more quality and reliability are required, making the validation of VLSI circuits more and more challenging Feng, [2]. The usage of integrated circuits is almost everywhere from kid's toys to highly equipped electronic machinery. Also, there is the extensive usage of digital ICs in the laboratories of colleges and universities where students learn how they work and learn to create the possible circuits and design applications using them. It is quite possible for the students to make mistakes at this stage and even one misplaced connection to the IC would lead to internal damage and the circuit may not work as expected. In research centers and educational institutions, users often only deal with a common range of digital ICs, which mainly are basic logic gates from the 74 series TTL, 40xx CMOS, Op-amps and 555 timer ICs. Different ICs

come with different specifications. Thus, it becomes imperative to apply different hardware configurations and feed all possible inputs for checking different ICs. This is not limited to research and educational institutions. Even in the industries, manufacturing defects are also unavoidable in manufacturing processes. Hence in the electronics industries, IC testing is vital to separate good IC chip from the bad. Generally, testing is proving the functional correctness of a product (Bushnell & Agrawal, [3]). It can thus be implied that testing of ICs refers to a series of tasks done to check the functionality of ICs. Integrated circuit testing is continuously improved by the evolution of design, manufacturing, packaging, and new applications. Testing not only contributes to design verification, but also is an important means for defect screening. It is an important constituent throughout the life cycle of ICs.

II. Review of Related Works

Integrated circuits form the backbone of modern electronics where they are used in manufacturing industries. Manufacturing defects are unavoidable in manufacturing process. Hence in the electronics industries, IC testing is vital to separate a good chip from the bad. In the industry, IC testing is often done using Automated Test Equipment (ATE) which are large, complex and very costly machineries. Likewise, at the consumer end, there are digital IC testers to perform testing on digital chips. Depending on the functionalities of the tester, the cost of a traditional digital IC tester usually comes at a price too high for an individual to own. These digital IC testers come in different specifications, normally defined by the range of ICs it can support.

To this end, a Field Programmable Gate Array (FPGA)-based reconfigurable digital chip tester was implemented by Fang *et al* [4]. The aim of this project is to achieve a reconfigurable, user friendly and cost-effective digital chip tester for users to perform chip testing on the most commonly used digital ICs. The project adopted the software-defined approach and was implemented on an FPGA which makes it versatile and reconfigurable. One advantage of this tester is it is able to test each output of a device individually which the traditional tester cannot perform. This will allow the user to still be able to use the functioning gates of a chip while avoiding the faulty ones, hence not putting the entire chip to waste. However, it was limited to the testing of 74xx series and as such had no facility for Operational Amplifiers and 555-timer ICs.

In 2011, Kiran Kumar [5] logic Integrated Circuit (IC) functional tester. The objective of the project was to develop a low cost, computer independent and user-friendly logic Integrated Circuit (IC) tester. The logic IC tester was able to test the function of basic 74 series TTL Logic gates (AND, OR, NOR, NAND, XOR, XNOR, Inverter (NOT)) and flip-flop ICs (D flip-flop, JK flip-flop). The logic IC functional tester can be operated in Personal Computer (PC) mode or Portable mode. This tester uses the flexible programmable features of PIC16F877A microcontroller for many applications. Visual Basic was used to develop the user interface to transmit the instruction from computer to the PIC16F877A microcontroller through Universal Serial Bus (USB) interface for PC mode. However, a limitation of this system was that it had no facility for testing Op-amps and the popular 555 timer IC.

Hemaet *al* [6] also implemented a Multiplexer Based Digital Integrated Circuit Tester. It can test digital ICs having 14 pins and as such was an improvement over earlier models implemented. This model applies the necessary signals to the inputs of the IC, monitoring the outputs at each stage and comparing them with the outputs in the truth table. Any discrepancy in the functioning of the IC results in a fail indication through LEDs. The testing procedure is accomplished with the help of keys present on the main board. Apparently, it still had no functionality for Operational Amplifiers and the versatile 555 timer ICs.

Selvarani.*et al.* [7] also implemented a Digital IC Tester for individual Gates on DIP Package using ATmega328p Microcontroller. The design methodology of the implemented device was the prototyping design approach. The implemented device was only optimized for logic gates and as such could not test analog Op-amp integrated circuits.

A Digital IC tester with embedded truth table was designed and implemented by Bhaskar&Rajib [8]. The device was able to test the CMOS 40xx and TTL 74xx series of ICs successfully. In this case, there was still no Op-amp and triple 555 timer IC testing facility.

Jenyfal *et al* [9] implemented an embedded digital IC tester for structural testing using Arduino micro controller. A distinct novelty in their design was the inclusion of a continuity and leakage test functionality. The result is low-cost automatic test equipment, able to execute a preliminary digital test, using just a laptop and an Arduino interfacing. It could handle different I/O combinations and could detect delay with the precision. It can both visually show the resultant voltage/current-time graphs and store them as text files. This novel and improved IC tester still had no provision for Op-amps and 555 timer IC testing.

Taweel and Mujahed [10] also designed and implemented a mobile-based digital IC tester. It consists of three main parts: IC socket, Android mobile, and website. The IC socket is built from connecting Arduino Nano and ZIF to test ICs. The Android mobile is connected to this socket via on-the-go cable to make it work as the main processor of the project. The website is created in order to add new unsupported ICs to the project's

database and verify coming user's packages from an Android application by JSON. Although a novel design, it had no facility for testing Op- amps and 555 timer IC.

Roberto and Anna [11] did a comprehensive review on static and dynamic characterization of digital circuits in CNTFET and CMOS Technology. In this paper, the researchers did review a procedure to characterize digital circuits in CNTFET and CMOS technology in order to compare them. To achieve this goal, a semi-empirical compact CNTFET model was proposed and the BSIM4 model for MOS device. This review covered the static and dynamic characterization of NAND gate and Full Adder, using the software Advanced Design System (ADS) which is compatible with the Verilog-A programming language. The obtained results allow to highlight the differences between the two technologies. Definitely the optimal results have been at 0.5 V and 50 GHz for CNTFET, while for CMOS technology at 3 V and 200 MHz.

III. Methodology

The methodology utilized in this dissertation was the bottom-up design method in which the system functionality was analytically broken down into sub-units for implementation before integration to implement the system. As such, the block diagram of the Improved Integrated Circuit Multi-tester is shown in Fig 1. It consists of the Integrated Power Supply unit, Negative Voltage Generating unit, Keypad Input unit, Control unit, Zero Insertion Force (ZIF) IC socket holder and Display unit.

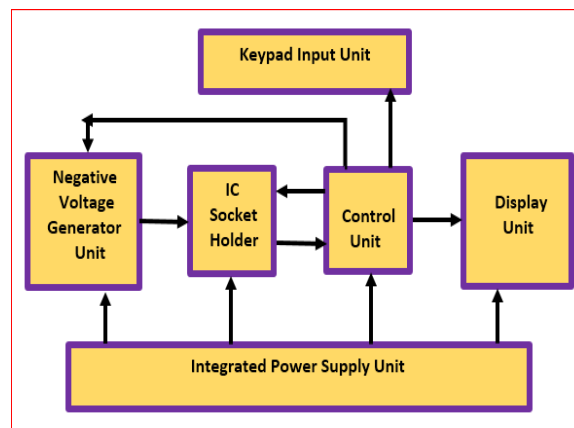


Fig. 1 Block Diagram of the Proposed System

A. Hardware Components

1. DC to DC Switching Converter

This is basically the type of voltage regulator most used in the power supply section due to its high efficiency and superb regulation. The term “switched mode converter” is used to describe a circuit which takes DC input (unregulated) and provides single or multiple DC outputs, again of same or opposite polarity and of a lower or higher voltage. The equipment for DC conversion can be divided into four technologies Alexander [12]. DC/DC Converters can be used to increase output voltage (boost conversion) or decrease (buck conversion) and/or reverse the voltage polarity at the output. Image of the LM256 DC to DC converter module is shown in fig 2.



Fig 2 LM256 DC to DC Voltage Converter

2. Keypad Input Unit

To provide a means for inputting the IC number to the microcontroller, a 4 x 3 keypad module was included in the interface to the control unit. It contains 4 rows and 3 columns. The keypad contains 12-buttons, somewhat like what is on a telephone. A 12-button keypad has 4 rows and 3 columns. Pressing a button will short one of the four row outputs to one of the three column inputs. From this input, the ESP32 controller can determine which button was pressed out of 12 buttons. For example, when key 1 is pressed, column 1 and row 1 are shorted together. The ESP32 will find out the button pressed, present in first row. Image the 4 x 4 matrix keypad module is shown in fig 3.

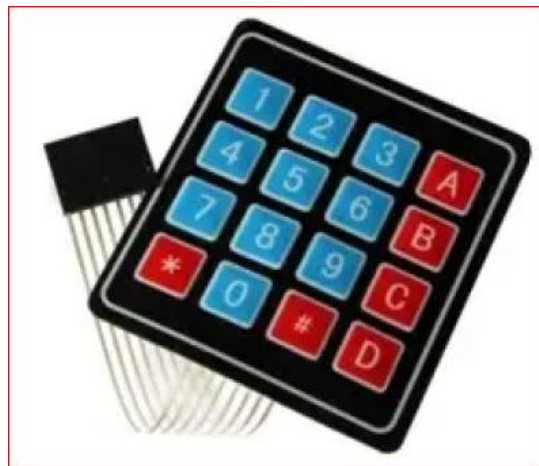


Fig 3. Image of The 4x4 keypad Module

When a button is pressed on the keypad module, the corresponding 8-bit ASCII code for the depressed button is sent to the control unit.

3. Main Controller (ESP-32 Microcontroller)

ESP32 is a series of low-cost, low-power system on-a-chip microcontroller with integrated Wi-Fi and dual-mode Bluetooth. The ESP32 series employs either a Tensilica Xtensa LX6 microprocessor in both dual-core and single-core variations, Xtensa LX7 dual-core microprocessor and a single-core RISC-V microprocessor and includes built-in antenna switches, RF balun, power amplifier, and low-noise receive amplifier, filters, and power-management modules. ESP32 is created and developed by Espressif Systems, a Shanghai-based Chinese company, and is manufactured by TSMC using their 40 nm process. It is a successor to the ESP8266 microcontroller. Image of the ESP32 microcontroller is shown in fig 4.

The microcontroller simply contains everything needed to support it and by connecting it to a computer with a USB cable and powering it with an AC-to-DC adapter or battery to get started.

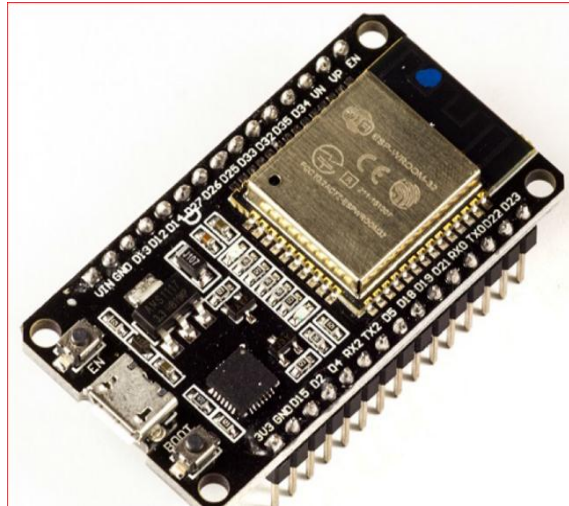


Fig. 4. Image of The ESP32 Microcontroller

The specifications of the ESP32 Dev Kit 1 is listed below

- I. Integrated Crystal– 40 MHz
- II. Module Interfaces– UART, SPI, I2C, PWM, ADC, DAC, GPIO, pulse counter, capacitive touch sensor
- III. Integrated SPI flash– 4 MB.
- IV. ROM– 448 KB (for booting and core functions)
- V. SRAM– 520 KB
- VI. Integrated Connectivity Protocols– WiFi, Bluetooth, BLE with On–chip sensor– Hall sensor
- VII. Operating temperature range—40 – 85 degrees Celsius and an operating Voltage– 3.3V

4. Display Unit

This unit consist of the Liquid Crystal Display (LCD). The LCD screen is used to display options of ICs that the user can select from and to also display the results of tests carried out on the IC under test. This is possible due to its data terminals and command register that the microcontroller is connected to. The LCD contains four lines and each line can display 16 characters and is known as 16 x 4 LCD. Image of a 16 x 4 LCD module is shown in Fig 5.

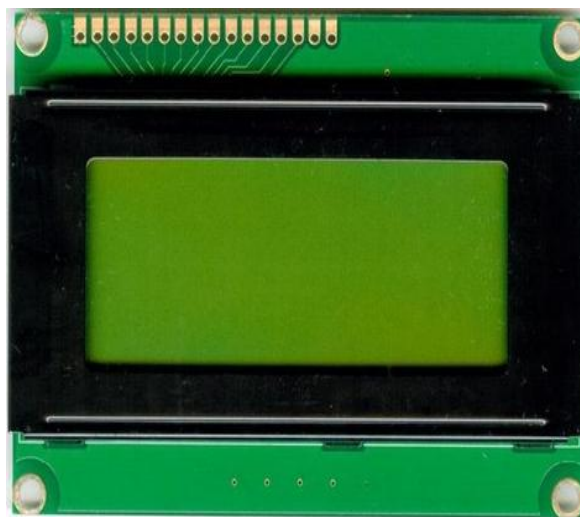


Fig 5. Image of The 4x4 keypad Module

5 Software Components

Programming Environment – The Arduino Integrated Programming Environment V2.2.1

1. Algorithm of the Proposed System

Start

Initialize all M, N, K and other variables.

Initialize input/output variables and LCD

Prompt user for IC Type
 Read input (M)
 If M = A, 555 Timer IC selected
 Configure output Pins
 Set power and GND pins
 Measure High and Low period of pulse
 Compute frequency of output Signal from 555 Timer IC
 Call Display Function and display Results
 return
 If M = B, Op Amp IC selected
 Configure /input/output Pins
 Set power and GND pins
 Apply input voltage and read output voltage
 Compute Gain of Op Amp IC
 Call Display Function and display Results
 If M = C, CMOS IC selected
 Configure input/output Pins
 Set power and GND pins
 Generate combinational Test signal for CMOS IC
 Read the results each input/output
 Call Display Function and display Results
 If M = D, TTL IC selected
 Configure input/output Pins
 Set power and GND pins
 Generate combinational Test signal for TTL IC
 Read the results each input/output
 Compare Results it with normal working IC signature in internal memory.
 Call Display Function and display Results
Stop.

6. Main Circuit Diagram

The complete circuit diagram of the system showing interconnections between the various units is shown in fig 6.

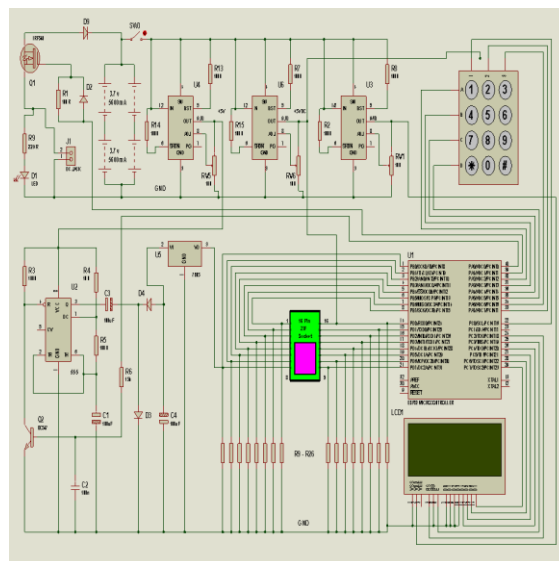


Fig 6 Main Circuit Diagram of Improved Integrated Circuit Multi tester

The system as shown in figure 6 shows overall circuit connection for logic IC functional tester. Four 3.7v 5600mA lithium-ion batteries constitute the power source for this logic IC tester. On board voltage regulators were used to reduce voltage level to become 5V to be used by ESP32 microcontroller and other peripherals. Main power switch used to control the power of the circuit either is turned ON or turned OFF. The

ESP32 microcontroller acts as the brain of the circuit. It controls the LCD, keypad, ZIF socket and sends and receives command.

The “upload” button on the Arduino IDE is used to download the program to the ESP32 microcontroller after the FTDI COM port is selected by going to device manager and looking for connected ports. Once a connection has been established and the program uploaded to the microcontroller, the “enable” button is used to reset the program. Thereafter, the device is switched ON and the display shows a list of files that represent IC that can be tested by the device. By default, the system when powered up displays the different IC test modes available, which are the 555-timer test mode, Operational amplifier test mode, CMOS test mode and the TTL test mode. This implies that that test files for each of the test modes are already programmed in the ESP32 microcontroller. This project comes with digital ICs: the 74xx, 40xx CMOS, uA741 Op-amp series and the 555 timer IC. Select one of the IC test modes in the list and place your IC in the 16 DIP socket with both pin 1s in the same place.

Four 3.7v 5600mA lithium-ion batteries constitute the power source for this logic IC tester. On board voltage regulators were used to reduce voltage level to become 5V to be used by the ESP32 microcontroller and other peripherals. Main power switch used to control the power of the circuit either is turned ON or turned OFF. The ESP32 microcontroller acts as the brain of the circuit. It controls the LCD, Keypad, ZIF socket and sends and receives command. In the CMOS and TTL testing mode, the system loads corresponding test files that contains the truth table for the particular type of IC selected. The control unit then used the truth table to generate the necessary logic signals that is applied to the inputs of the IC under test while the output pins are simultaneously sampled for response. The corresponding patterns read from the output of the CMOS or TTL IC is compared with the expected output pattern stored in the system’s internal memory. If the received pattern matches that stored internally, the IC under test is declared good. Otherwise, the IC is declared bad. In the 555 timer IC testing mode, the inserted 555 timer IC is configured as an astable (free running square wave signal generator) multivibrator with internal precision resistor R and C while the output frequency of the 555 timer IC is sampled and compared with the expected frequency calculated internally. With tolerance factors of R and C taken into consideration, the output frequency from the IC under test should not deviate from an expected range of value which if within, the 555 timer IC under test is declared good. Otherwise, its declared bad. A similar concept is followed in testing Operational amplifier. When test mode selected is Op-amp, the IC under test is configured as a non-inverting amplifier with a gain given by $\text{Gain} = 1 + (R_f/R_i)$. Two input voltages of 0.5v and 1.5v is sequentially applied to the input terminals of the Op-amp IC under test while the output is sensed and measured by the control unit. This value is the divided by either of the input voltages to give the real gain which is then compared with the gain from the resistors. If the measured value deviates from this value by a certain margin, the Op-amp is declared bad.

7 Results and Discussion

This section shows the results from tests carried out on the Improved Integrated Circuit Multi-tester and other conventional IC testers taking into cognizance the speed of processing test result and the percentage error of measurement.

Results of 555 timer IC

The results obtained from testing different 555 timer IC with the implemented system is shown in table 7.1.

Table 7.1 Table Showing Test Results for the Improved IC tester and an external 555 Timer IC Tester

S/N	No of 555 Timer ICs	Existing IC Tester			Improved IC Multi-tester			IC Status
		Measured Frequency (1kHz)	Frequency deviation	Percentage error (%)	Measured Frequency (1.30kHz)	Frequency deviation	Percentage error	
1	1 st 555 Timer IC	1023.11	23.11	2.25 %	1315.10	8.09	0.6%	Good
2	2 nd 555 Timer IC	989.43	10.57	1.07%	1308.28	1.27	0.097%	Good
3	3 rd 555 Timer IC	1067.67	17.67	1.66%	1298.32	8.69	0.67%	Good
4	4 th 555 Timer IC	1015.52	15.2	1.49%	1298.70	8.31	0.64%	Good
5	5 th 555 Timer IC	1084.21	84.21	7.77%	1367.54	60.53	4.43%	Bad
6	6 th 555 Timer IC	1012.01	12.01	1.19%	1310.70	3.69	0.28%	Good
	7 th 555 Timer IC							

7	8 th 555 Timer IC	1019.34	19.34	1.89%	1298.67	8.34	0.64%	Good
8	9 th 555 Timer IC	1020.16	20.16	0.098%	1310.71	3.7	0.28%	Good
9	10 th 555 Timer IC	937.15	62.85	6.70%	1250.72	56.29	4.5%	Bad
10		1017.23	17.23	1.69%	1308.44	1.43	0.11%	Good

Fig 7. Line graph showing comparison between percentage error of the existing IC tester and the Improved IC Multi-tester

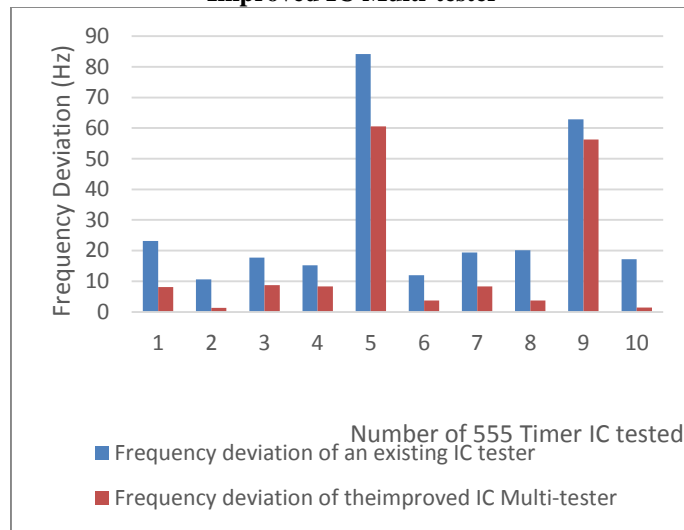
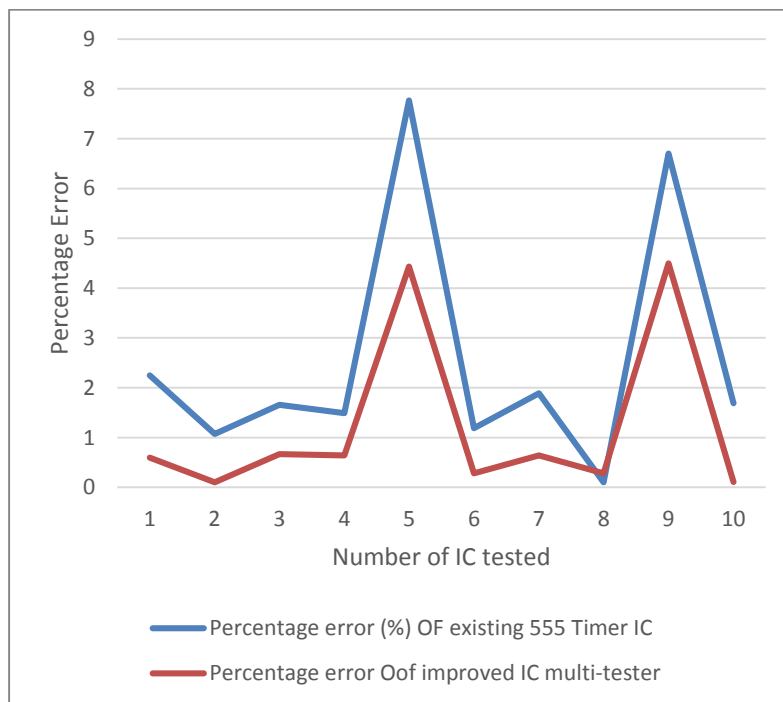


Fig 8. A bar Chart plot of Frequency deviation of the Improved IC Multi-tester and an external 555 timer IC Tester



7.1 Results of Operational Amplifier Integrated Circuit

The results (in gain) obtained from testing a total of 4 different types of Op-amp IC with the Improved IC Multi-tester and a generic Op-amp Multi-tester (TDA2001) is shown in table 7.2,

Table 7.2. Table Showing Measured Gains for Different Op-Amp ICs using Generic Multi Op Amp Tester TDA2011 and the Improved Integrated Circuit Multi-Tester.

S/N	Operational Amplifier Type	IC Status	Improved IC Multi-Tester	Generic Op-Amp Tester TDA2011
1	LM358 Operational Amplifier	Good	3.3	3.5
2	uA741 Operational Amplifier	Good	3.07	3.5
3	CA3140E Op-Amplifier	Good	3.2	3.5
4	CA3130 Op-Amplifier	Bad	2.4	2.7



Fig 9. One of the results of Testing Op-Amp IC with the Improved IC Multi-Tester.

7.2 Results of 4071 CMOS Integrated Circuit.

One of the results obtained from testing a 4071 CMOS IC with the Improved Integrated Circuit Multi-tester is shown in fig 10.



Fig 10 One of the results of testing 4071 CMOS IC with the Improved IC Multi-Tester.

7.3 Results of 4001 Transistor-Transistor Logic (TTL) Integrated Circuit

One of the results for Transistor-Transistor Logic (TTL) test is shown in fig 11

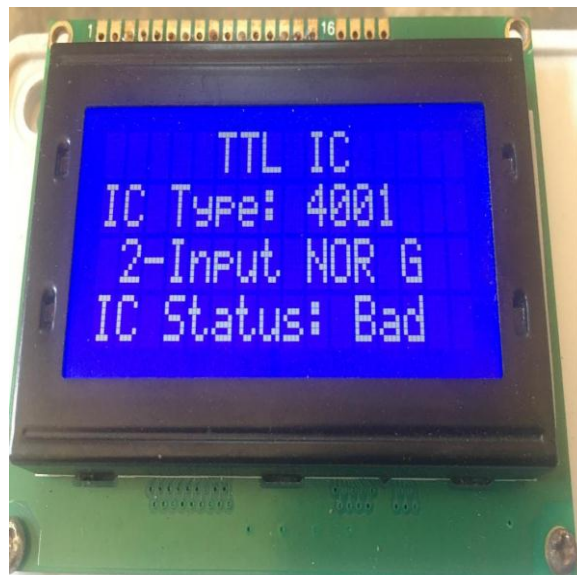


Fig 11 One of the results of testing 4001 TTL IC with the Improved IC Multi-Tester

VIII. Discussions of Findings

The Improved IC Multi-Tester is implemented by using the ESP32 microcontroller. The processing of the inputs and outputs is done by the microcontroller. The display part on the microcontroller board is implemented using LCD. After the successful testing of the ICs, the result is displayed on the LCD. A total of four ICs were tested starting with a 555 timer IC. The results displayed for the 555 timer IC showed a detected and average measured frequency of 1306.18Hz which is within the range of expected frequency ($\pm 3.4\%$ of 1307.1Hz) for a good and working 555 timer IC.

The results displayed for the uA741 Operational amplifier timer IC showed a detected and measured gain of 3.07 which is within the range of expected gain ($\pm 5\%$ of 3.3) for a good and working Op-amp IC. A CMOS 4071 and a 4001 TTL IC were tested. The CMOS 4071 IC was declared good by the system while the 4001 TTL IC failed the test and was declared bad by the system. Further results showed the different time taken to test each category or type of IC that the system is designed to test. It can be observed that while it takes less than one second to test CMOS and TTL integrated circuits, it takes about 2 seconds to test the 555 timer IC and about 3.2 seconds to test the Operational amplifier. This is perfectly normal due to the different sequence of voltage application to the input of the Operational amplifier so as to compute the gain.

IX. Conclusion

In today's 21st century, there is a constant strive to achieve improvements in cost effectiveness and time efficiency when it comes to the troubleshooting and testing of integrated circuits. This is said against the backdrop that integrated circuits have become the main stay to today technological revolution. From complex integrated system of space exploration to dynamic industrial control systems, residential control systems and even sophisticated toys for kids, the role and number of integrated circuits utilized is so enormous that it cannot be quantified. In view of the fact that components can go bad after unprofessional handling, shipping and even manufacturing defects (since no production or manufacturing process is perfect or fault free), the need for testing of integrated circuits becomes a necessity. Although quite a lot of IC tester devices are available, most are as expensive as to be out of reach of students and do not have the facility for measuring 555 timer ICs and Operational Amplifiers.

In this dissertation, an Improved IC Multi-tester has been proposed and designed and developed using the bottom-up approach. It comprises a 4x4 matrix keypad for input, a ZIF (zero insertion force) socket, an ESP32 microcontroller, an integrated power supply unit and 16x4 LCD display. This instrument provides a practical approach to addressing the problem of wasting unnecessary time while troubleshooting faulty ICs or testing ICs to be used in a circuit. It has the advantage of being able to test various types of ICs like the popular

555 timer IC, Operational Amplifiers, CMOS ICs and TTL ICs. This will no doubt allow end users of these aforementioned integrated circuits to still be able to sift good and working ICs from faulty ICs. Due to its re-configurability and expandability, it is proven to be a more cost-effective solution in the long run comparing it to a traditional digital chip tester that is not reprogrammable. After the several months of development and debugging, finally the project has been successfully completed. The project's aim and the main objectives have been accomplished. The Improved Integrated Circuit Multi-Tester is able to test basic logic gates of CMOS and TTL categories in 14 pins. Arduino Integrated development environment was utilized in the programming of the ESP32 microcontroller in conjunction with a 4x4 matrix keypad for input commands to the system. This project hopes to bring forth a notable resource for future development in the field of software-defined test approach.

Reference

- [1]. D. Y. Lee, D. D. Wentzloff, and J. P. Hayes, "Wireless Wafer-Level Testing of Integrated Circuits via Capacitively-Coupled Channels," in Proc. IEEE DDECS, pp. 99-104, Apr. 2011.
- [2]. B. Feng, Research on Optimization Method of Low Power Design for Analog-Digital Mixed Signal Circuit Testing (Guilin University of Electronic Technology, Guilin, 2012)
- [3]. M. L. Bushnell and V. D. Agrawal, Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits, Springer, 2000.
- [4]. Fang pang; Brandon, T.; Cockburn, B; Hume, M (2004) A reconfigurable digital IC tester implemented using the ARM integrator rapid Prototyping System. Electrical and Computer Engineering, ,IEEE.
- [5]. Kiran Kumar Kolli, Implementation of IC Tester, GayatriVidhyaParishad College of Engineering, JNTU, Visakhapatnam.
- [6]. Hema Thota1, Sridhar Sammeta2, Prudhvi Raj Thota (2015) Multiplexer Based Digital Integrated Circuit Tester. International journal of innovative research in electrical, electronics, instrumentation and control engineering Vol. 3, issue 4,
- [7]. Mrs.Selvarani. A, Manimegalai.K Premalatha.G Priyadharshini. (2017) Digital IC Test for Individual Gates on DIP Package Using ATmega328p Microcontroller
- [8]. BhaskarJyoti Borah & Rajib Biswas.(2016) "Digital IC tester with embedded truth table".Electronics for you.
- [9]. Jenyfal Sampson, M.Anusha, S. Rajeswari & B.A. Anoohya (2021) Embedded Digital Ic Tester For Structural testing Using Arduino Micro Controller. International Journal of Creative Research Thoughts (IJCRT) Volume 9, Issue 5 May 2021 | ISSN: 2320-2882
- [10]. Alexander Miczo. "Basic Tester Architectures," in Digital Logic Testing and Simulation, 2nd ed., New Jersey: John Wiley & Sons, Inc., 2003, pp. 284.