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Fabrication of field-effect transistor based on RGO

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ABSTRACT:*Field-effect transistors with graphene (GFETs) as the conducting channels are under investigation as promising chemical and biological sensors. In order for graphene to fulfill this promise and become a material for the large-scale manufacture of high-performance electronics, large-area, high-quality graphene on substrates amenable to electrical device operation and sensors fabrication is needed. So the purpose of this paper is to provide in detail how reduced graphene oxide suspension (100μg RGO/ 1ml NMP) was developed, and functionalized the back gate FETs. Following an introduction, we report a solution-based method that allows uniform and controllable deposition of reduced graphene oxide thin films ranging from a single monolayer to several layers in thicknesses between the electrodes in FET. The Raman spectrum of graphene consists of a number of peaks which are well characterized and understood. Electrical transfer property tests revealed that both of the two FETs exhibit V-shaped ambipolar field effect behavior from p-type region to n-type region. This research investigared the preparation of back gate field effect transistor with reduced graphene oxide via a low-cost manufacturing method. The reasults suggest that our method is fast, facile, and substrate independent.*

Keywords: *Graphene Oxide; Back gate FETs; Suspension; SEM; V-shaped ambipolar*

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I. INTRODUCTION

Nanostructured carbon materials are well-known for their excellent capability to store energy. Graphene, a single-layer of carbon atoms densely compacted into a two-dimensional honeycomb crystal lattice, has attracted tremendous attention in recent years, because of its unique electronic, optical, thermal, and mechanical properties [1]. It provides a variety of novel applications such as field-effect transistors (FETs) [2] , ultrasensitive sensors [3], transparent electrodes, and novel nanocomposites [4]. Graphene is particularly advantageous in biosensing, transparent conducting electrodes, electronic devices [5] and sensors due toits large detection area, high charge mobility, low noise,and biocompatibility [6]. Graphene can be synthesized by various methods such as chemical vapor deposition, mechanical exfoliation and cleavage, and it can also annealing a single-crystal SiC under ultrahigh vacuum [7]. These methods, however, have many drawback including high energy requirement, low yield, and limitation of instrument. Up to now, the chemical method has become a promising route to produce graphene sheets, though graphene derived by this method could contain a significant amount of oxygen functional groups and defects. This is because it is simple, inexpensive, and suitable for large-scale or mass production. The process involves 3 important steps: graphite oxidation, exfoliation of graphite oxide, and reduction of graphene oxide sheets. In the first step, bulk graphite would be oxidized by chemical oxidation to become hydrophilic graphite oxide (GO). Graphite oxide is then exfoliated into monolayers or few-layered stacks of graphene oxide (XGO). This could be achieved by various thermal and mechanical methods. Sonicating or stirring in water is the most commonly used method. Finally, graphene oxide is reduced into graphene-like material. Previous works have reported the reduction by using reductants such as hydrazine. Liao et al. [8] for example, have reported a new simple, nontoxic and hydrazine-free method to reduce graphene oxide by stirring in hot water under acid condition. GFETs are widely applied in physical, chemical and biological sensing field. In this article, we aim to show the integration between the preparation and

characteristics of the newly developed materials, and represent the sensing applications of GFETs in physical, chemical and biological territory. In this paper, we first treated graphite powders with concentrated sulfuric and potassium permanganate, using modified Hummer's method, to produce graphite oxide. The process was designed to be simple and with a low risk, so that it can be done in collage's laboratory. Graphite oxide was then exfoliated and reduced into reduced graphene oxide (RGO) by ultra-sonication in water and stirring in hot water. The obtained samples were studied by FTIR, Raman spectroscopy, SEM and TEM methods.

II. EXPERIMENTAL SECTION INTRODUCTION

2.1 Materials

Hydrogen peroxide (30 wt %), Sulfuric acid (95%), (3-Aminopropyl) triethoxysilane (A3648-100ML) APTES and N-Methylpyrrolidone (NMP) were obtained from Sigma-Aldrich and used as received.

2.2 Fabricating transistor

In order to fabricate field effect transistor, p-type $< 100 >$wafer with a thickness of $400^{\mu m}$available in the laboratory with $30^{\Omega/Cm}$ resistance properties were used. Wafers are cut in $1.5^{cm} \times 1.5^{cm}$ dimensions. To clean the samples we use RCA method, 2 part H_2O ‹2 part NH_4OHand2 part H_2O_2solution. The provided solution was put on heater with $80 \pm 5^{\circ C}$ temperature and the samples in it were submerged for 15 minutes. Then, wash the samples in a deionized water container for 10 minutes at ambient temperature. And finally, samples are exposed to wind and clean them. For oxide deposition on one side of the samples, we put them on a clean alumina device and place them in oxidation furnace. For depositing 350^{nm} oxide, the dry oxidation method in $1000^{\circ C}$ is used. Oxygen flow in the dry oxidation is set at about 5^{Sccm} . It should be noted that, quality oxide layer affect sensor performance.

III. DESIGNINGMARKERSMASKAND DEPOSITION ALIGNING MARKERS

The utilized pattern is designed with marker mask for aligning in photolithography processes such as graphene sheets Patterning, deposition of electrodes as shown in figure 1. The Cr electrodes (30^{nm} Cr) [9] with $W = 30^{\mu m}$, $L = 56^{\mu m}$ and $W = 60^{\mu m}$, $L = 56^{\mu m}$, were fabricated on Sio2 (300 nm)/Si substrate to make aligning markers using conventional macro-Nano processing technologies including photolithography, lift-off process and electron-beam evaporation. A large area between the electrodes markers due to locating to part of the graphene sheets created under the electrodes, in order to get a better connection between the source and drain electrodes as is shown in Figure 2. Figure 1 shows Optical microscopy imagessamples of creating markers. Figure 3shows SEM images of the markers electrodes.

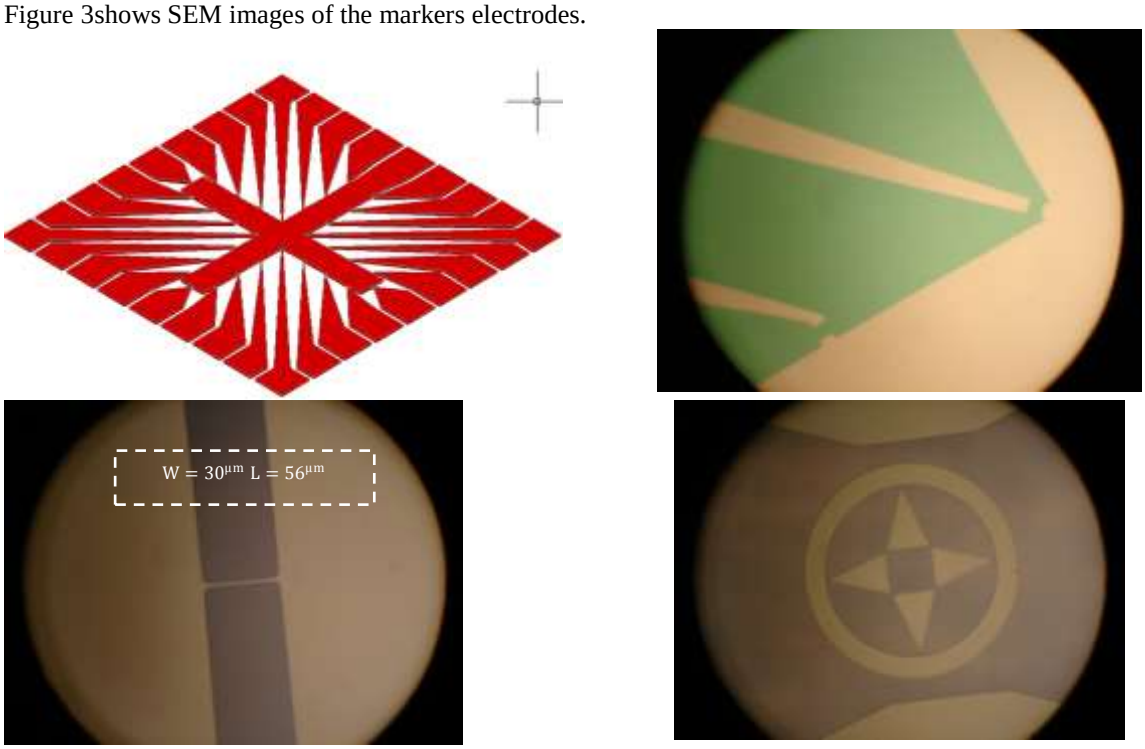

Figure 1: Markers Mask (Top Row), Optical Microscopy Imagesof The Aligning Markers Electrodes (Bottom Row).

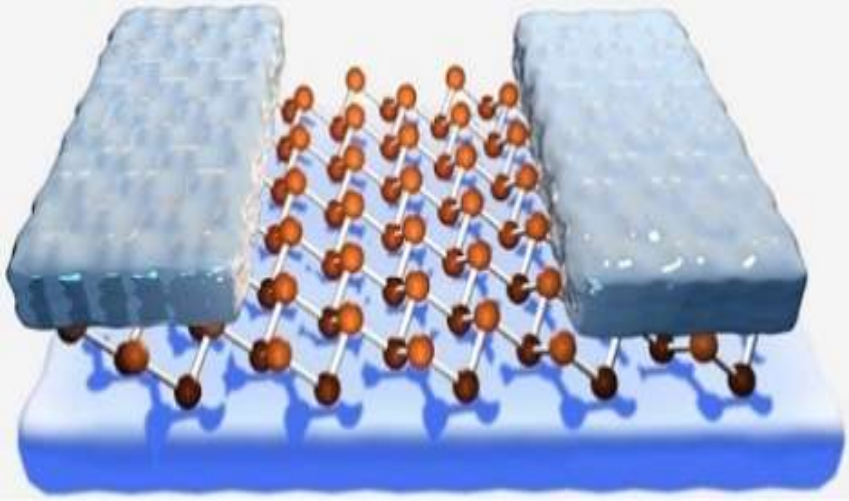

Figure 2: The part of the graphene sheets under the electrodes.

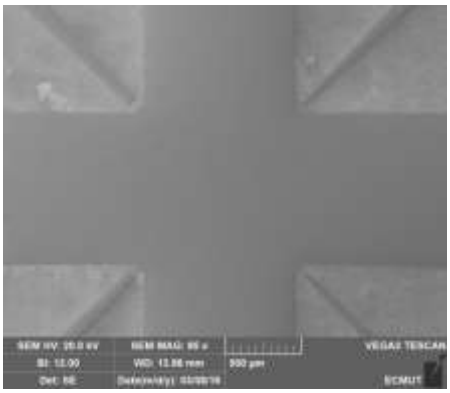

Figure 3: The SEM images of the markers electrodes (30^{nm} Cr onSi/Sio_2) after lift-off process.

IV. PREPARATION OF RGO SUSPENSION

To prepare the RGO suspension, 100 µg RGO powder was added in NMP (1 ml) [10] and sonicated for 2 hours, then the suspension at a speed of 8000 rpm for 20 minutes was centrifuged, and the supernatant was kept for the next stage (small sheets of RGO), and low volume suspension (large sheets) to be discarded. Then the suspension at a speed of 1500 rpm for 20 minutes was centrifuged, and sediment at the bottom of the tube was kept, the final volume 1.5 ml was reached, resulting in a transparent, black, and stable RGO suspension (100 µg RGO/1 ml NMP).

V. SUBSTRATE PREPARATION AND DEPOSITION OF RGO SUSPENSION

To prepare the wafer to apply the RGO suspension to form a sheet of graphene, surface must be prepared, for this purpose, Piranha and APTES solution is used to activate the surface .Piranha solution, also known as piranha etch, is a mixture of sulfuric acid (H2So4) and hydrogen peroxide (H2O2), used to clean organic residues off substrates. Because the mixture is a strong oxidizing agent, it will remove most organic matter, and it will also hydroxylate most surfaces (add OH groups), making them highly hydrophilic (water-compatible). Piranha solution must be prepared with great care. It is highly corrosive and an extremely powerful oxidizer. Surfaces must be reasonably clean and completely free of organic solvents from previouswash steps before coming into contact with piranha solution. Piranha solution should always be prepared by adding hydrogen peroxide to sulfuric acid in a slowly way, the reverse must be avoided. Mixing solution is extremely exothermic. Piranha solution is used to make glass hydrophilic by hydroxylating the surface, thus increasing the number of silanol groups on the surface. Silicon wafer (Si/Sio_2) was cleaned in piranha solution (3:1 H_2OSO_4:H_2O_2 mixture, caution extremely corrosive and highly exothermic) for 10 min followed by extensive rinsing with deionized water, dried under a nitrogen stream before APTES deposition, and stored in a vacuum oven at 80 °C until use, typically within a period of 2h. A general consensus regarding the 3-Aminopropyltriethoxysilane (APTES) film formation on a silicon substrate is that silanization begins with the hydrolysis of ethoxy groups in APTES, a process catalyzed by water, leading to the formation of silanols . Two types of solvents, anhydrous toluene (water < 30 ppm) and phosphate-buffered saline (PBS, pH 7.2 +/-0.1,

and ionic strength 10 mM), were used to prepare APTES solutions with a concentration of 2.0%. APTES films were prepared by incubating clean silicon wafers in APTES solutions for 3 h. After the controlled deposition, silicon wafers were sonicated twice in APTES-free solvents for 10 min to remove loosely physisorbed APTES. An APTES solution is very sensitive to the humidity and ambient gases .So the process of APTES in the presence of nitrogen gas is done by the setup Figure 4a and reduced graphene oxide suspension is shown in Figure 4b.

Figure 4: a) The process of activating the surface ($Si/Sio_2/Cr$ markers/Piranha) with APTES solutions. b) Reduced graphene oxide suspension.

To prepare RGO thin films, the diluted R-GO suspension was a spin-coating at 3000 RPM for 45 s onto the ($Si/Sio_2/Cr$ markers/Piranha /ATPES) substrate. After that, the R-GO FET was immersed in the Piranha solution and sonicated for 30 s to obtain few-layer R-GO, followed by thorough washing with DI water and drying with nitrogen, and thermally annealed at $150^{\circ C}$ in order to remove all solvent. The scanning electron microscopy (SEM) and Energy Dispersive Spectroscopy (Eds) map images of the R-GO sheets are illustrated in Figure 5. EDS map shows that there are no impurities on the surface, and only carbon and silicon.

SEM and Optical microscopy imagesof the $Si/Sio_2/Cr$ markers/Piranha /ATPES/RGO suspension with residual particles are shown in Figure 6. At this stage of the manufacturing process, graphene sheets were created on the intended sample. To use them as a channel of the transistor, graphene sheets must be patterning [11]. Its details in the next section explained.

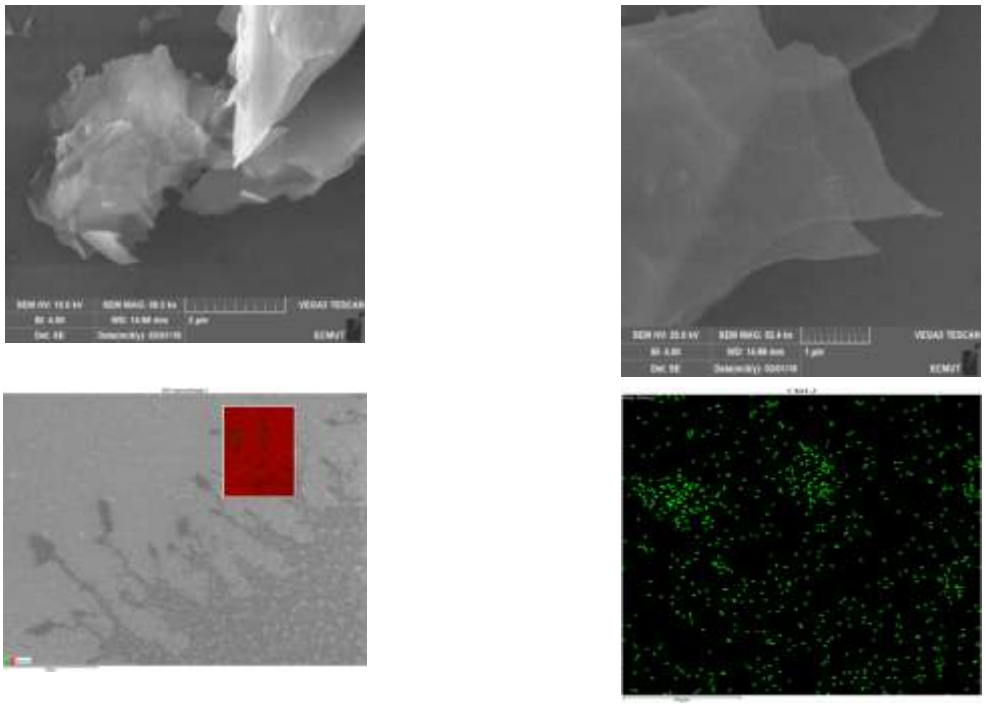

Figure 5: The SEM images of the RGO sheets deposited on a silicon wafer ($Si/Sio_2/Cr$ markers/Piranha / ATPES/RGO suspension), and Energy Dispersive Spectroscopy map.

Figure 6: The SEM and Optical microscopy images of the device Si /Sio_2/Piranha /ATPES/RGO suspension with residual particles.

VI. GRAPHENE PATTERNING MASK

Graphene patterning mask, with rectangles equal to the area between the electrodes in the markers mask is designed. Graphene patterning mask with the SEM images as shown in Figure 7. To apply graphene markers, (Rectangular $60 \times 56^{\mu m^2}$&$30 \times 56^{\mu m^2}$) were fabricated using conventional photolithography process and O_2 plasma (RIE) [12] for 10 minutes, with power 25w,$O_2 = 25$ Sccm, 350 mtorr pressure in order to removing the graphene sheets without the photoresist coating. Figure 8 shows samples of creating markers with photoresist coating on Rectangular $60 \times 56^{\mu m^2}$&$30 \times 56^{\mu m^2}$and SEM images of graphene markers. According to the SEM images above, below rectangles covered with photoresist the remaining graphene sheets, and the rest is destroyed by oxygen plasma.After patterning the graphene sheets with a corresponding mask and kept sheets in between the electrodes marker, clean the photoresist with acetone. Now, in this stage of the manufacturing process RGO-FET, graphene sheets are located between the electrodes and the other places are empty of the graphene sheets.

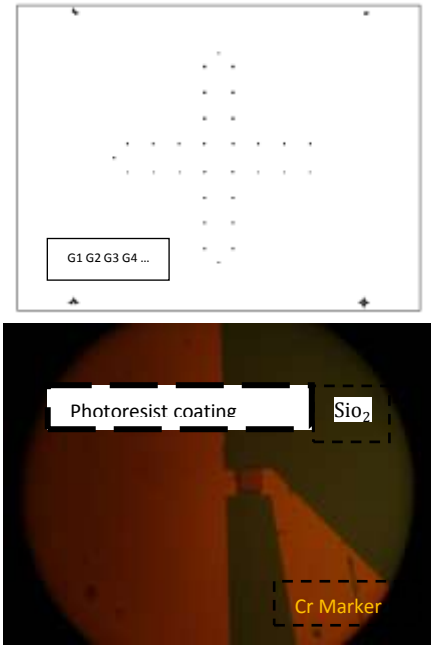

Figure 7: Graphene patterning mask, SEM images of graphene mask, to protect graphene in RIE process with photoresist (G1, G2, G3 and G4) (Upper row), Optical microscopy imagesof Cr markers with photoresist coating on rectangular places (Where the graphene sheets must be protected).

VII. Deposition of the Source and Drain electrodes

The utilized pattern is designed, which have 31 transistor samples with different dimensions. The fabrication of the RGO-FETs was completed by using the standard semiconductor technology. The gold electrodes (70^{nm} Au on 30^{nm} Cr) with $W = 30^{\mu m}$, $L = 6^{\mu m}$ and $W = 60^{\mu m}$, $L = 6^{\mu m}$, were fabricated on (Si /Sio_2/Cr markers/ graphene sheets) substrate, to make source and drain electrodes using conventional macro-Nano processing technologies including photolithography, lift-off process and electron-beam evaporation. The size of the whole device is1.24×1.24 mm^2. The electrodes (100 nm thick) are $L = 6^{\mu m}$ apart. To enhance the adhesion between the Au and the Si wafer, a 30 nm thick Cr layer was used. The (SEM) images of the RGO-FET with Cr-Au

electrodes are illustrated in Figure 8. Thus RGO-FET was created by applying masks and microelectronics processes.

I. RESULTS

A. Determine the number of layers in graphene using a Raman microscope

A Raman microscope is located at University of Tehran.Its laser power and its wavelength are 5 mW and 514.5 nm, respectively. If the laser power is more than 5 mW, it is possible for graphene to be burned. The Z scan is used to focus the laser on the sample surface. The peak position and height of the Raman spectra are known to depend on the number of layers in graphene [13], [14]. We found that we could successfully get single layer, six layer and multilayer graphene by mechanical cleavage, by comparing our data with that in Ref. [13]. The Raman spectrum of the R-GO is shown in Figure 9. The Raman spectrum was conducted directly on an R-GO sheet on the SiO2 /Si substrate at room temperature. The spectrum displays the D band at 1315 $cm^{-1}$and the G band at1579 cm^{-1}.

B. *Bipolar property of GRFET*

Bipolar property in GRFET structure refers to the passing of current by electrons in a range of gate voltage and by holes in another range of gate voltage [15]. Figure 10 shows bipolar conductance in device with $\pm 0.1^{v}$drain source voltage. It means that by increasing source gate voltage from minus amount to about half of drain source voltage, the role of hole carriers in conducting the current decreases gradually; and by increasing voltage to more than half of drain source voltage electrons function as major carriers in transmission of current. Now this comparison between the simulation and experimental results reveals high performance of GRFET.

C. *Characterization of Back-gate Devices*

We fabricated the RGO-FET devices based on the methods described in the manuscript. Figure 11 shows the image of the RGO-FET. The device is composed of 31 individual sensor arrays connected with the orresponding electrical lines and pads. Inset image shows the 31 pairs of electrodes, and the electrodes channel is 6 μm.

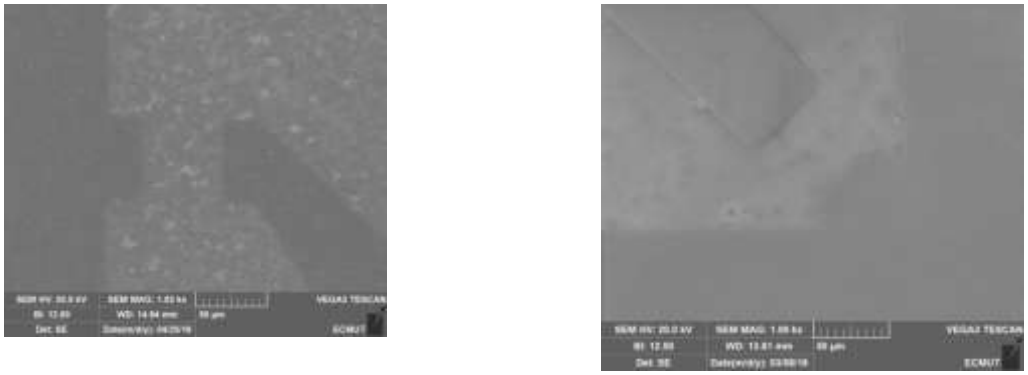

Figure 8: The SEM image of the device (RGO-FET) with single R-GO sheet spanning across Au electrodes. ,(Si/Sio_2/Cr markers/ Piranha /ATPES/RGO/Cr/Au)

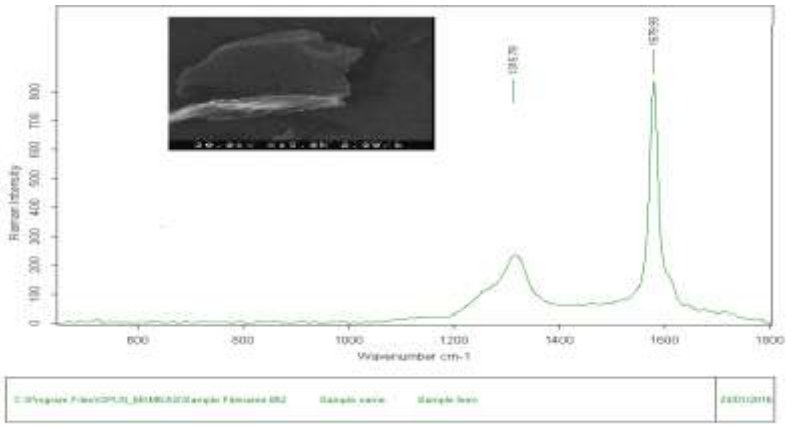

Figure 9: Raman spectrum of the R-GO.

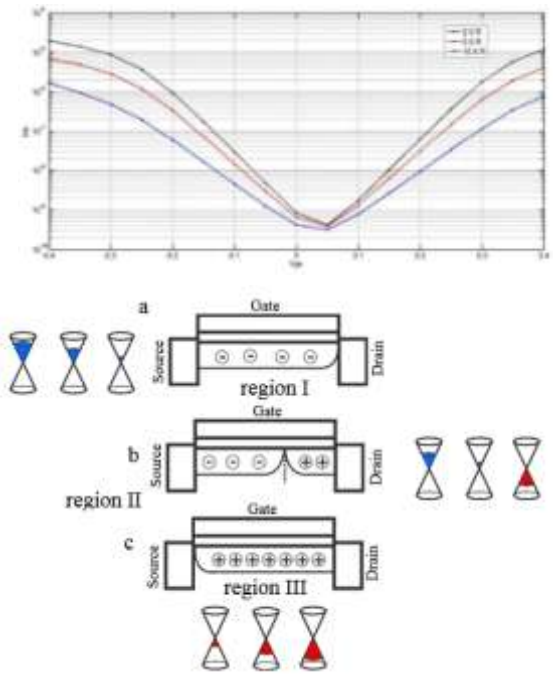

Figure 10:a) The transfer characteristics of transistor with a width of $6^{\mu m}$, V-shaped ambipolar FET. b) Energy band diagram for an ambipolar characteristic of GR-FETs depending on whether $V_g, > 0$ or$V_g < 0,$VDS. Assuming that VDS > 0, in region I, the device has n-type carriers everywhere in the channel. In region II, the device has n-type carriers at the source side of the channel and p-type carriers at the drain side of the channel. This is the ambipolar region.

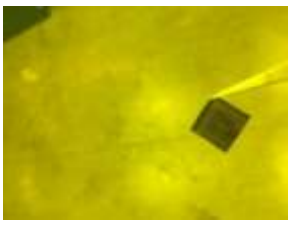

Figure 11: The image of the RGO-FET device.

The back gate devices were ready for electrical measurement. This shows that RGO-FETs are good candidates for transducers in liquid phase and gas sensors [16]. The back-gated R-GO FET devices were measured in a semiconductor parameter analyzer (4145B) coupled with a probe station. For $I_{ds} - V_{ds}$ curve measurements of the GFET devices, silver adhesive were used for connections, and a variable gate voltage was applied. To investigate the electrical properties of the R-GO FET device, the output and transfer characteristics of the R-GOFET were obtained prior to the functionalization of the R-GO. As shown in Figure 12, the typical $I_{ds} - V_{ds}$ curves were obtained to further examine the electrical characteristics of the R-GO FET device.

Figure 12: Electrical Properties of RGO-FET devices .$I_{ds} - V_{ds}$ output characteristics of the R-GO FET device with $\frac{W}{L} = 10$ electrodes. a) The gate voltage (V_g) is varied from 0 to 0.4 V with an interval of 0.2 V. b) The gate voltage (V_g) is varied from 0 to 0.7 V with an interval of 0.1 V.

The drain-source current decreases with a slight reduction of the gate voltage, indicating that the device reaction is sensitive to the gate voltage. I_{ds} Curve versus various gate voltages, i.e.V_g, for constant drain-source voltageis depited in Figure 13. From the $I_{ds} - V_g$ curve in Figure 13a, the p-type characteristics could be clearly observed at a small range of gate voltage (from - 5 to 0 V) under ambient conditions. As it was expected, the drain current is modulated almost symmetrically with back gate voltage. Electrical transfer property tests revealed that both of the two FETs exhibit V-shaped ambipolar field effect behavior from p-type region to n-type region ($V_g - 5$ to 5 V, $V_{ds} = 0.1$ V), as shown in figure 13b.

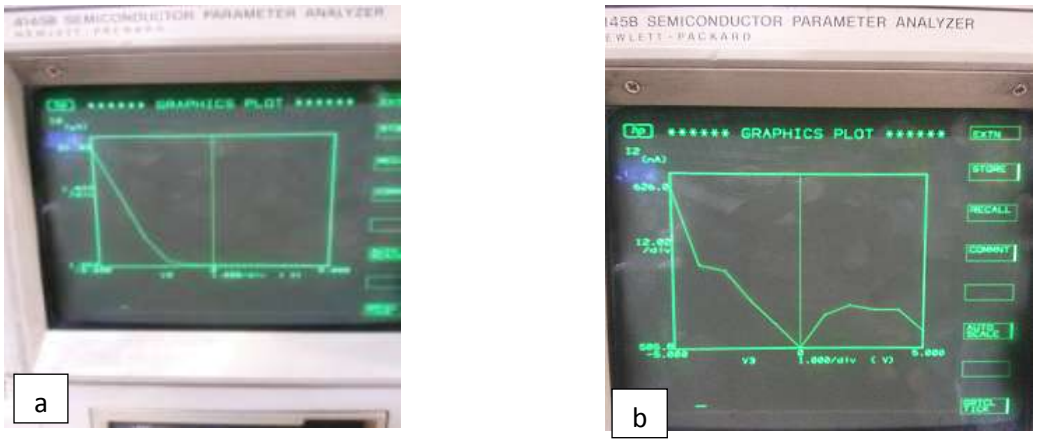

Figure 13:a) Electrical Properties of RGO-FET devices.$I_{ds} - V_g$ curve of the bare R-GO on a SiO2 /Si substrate ($V_{DS} = 0.1^v$). b) Back gate transfer characteristics of GFET.

Current measurements between terminals source and drain electrodes with $\frac{W}{L} = 10$ overlap very well. The hysteresis of the $I_{ds} - V_g$ curve between electrodes with $\frac{W}{L} = 10$ are small. The gate leakage current was in the nA range for all measurements as shown in figure 14a. Figure 14b illustrates the drain current as a function of source-drain voltage from -2.5 V to +2.5 V for various gate voltages. The drain currentlinearly increases with source-drain voltage which is a typical behaviour for GFETs at low bias. Also, it can be seen in this figure that conductivity (the slope of the lines) varies in agreement with transfer characteristics in figure 15b. When looking at the output characteristics, adeviation from zero point is observed; there is some amount of current at zero bias in all back gate voltages. Considering the low leakage current in the order of 2 nA, it seems that this effect is an offset error originates from measurement tool precision. We only include devices where all 18 terminals are working as "good devices" making the apparent yields (60 %). These results indicate that the graphene sheet is very clean and the graphene quality in the entire device channel is very uniform.

Figure 14: a) The gate leakage current b) Typical I-V characteristics of several GOFET devices. Output characteristics show linear behavior in the low-field regime.

II. CONCLUSIONS

In this paper, first, the RGO-FET device is fabricated on a Si/Sio_2substrate by the conventional macro-Nano processing technologies. Field effect transistor with continuous RGO stripes as micropatterned conductive channels were fabricated and some of the important and sensitive parameters of the field-effect transistor with RGO were simulated. To prepare the RGO suspension, 100 µg RGO powder was added in NMP (1 ml). Graphene sheets are controllably placed between electrodes by spin coating of suspension of RGO and microelectronic method. SEM show the structures of RGO, which are very thin sheets even through there is evidence of sheet folding. The RGO sheets were selectively deposited onto the electrodes by a self-assembly method and were thermally annealed to enhance their contact with the Au electrode. This technique provides a high success rate of fabricating GFETs with a flexibility of controlling the RGO alignment direction and the graphene sheets length. R-GO as the conducting material shows the obvious ambipolar characteristics at a small range of gate voltage on the back-gated FET devices under ambient conditions, and the devices are highly responsive to the low gate voltage. Using RGO band gap as the channel for RGO-FETs is represented as having great importance in measuring high on/off rate. In maximum currents, the channel levels resulting from drain source connections is not noticeable. Moreover, the resulting RGO shows p-type semiconductor behavior under ambient condition and can be directly used to fabricate high-performance electronic devices, such as gas sensors. Design and manufacture of explosives detector sensors based on GFET with biological receptor such as DNT receptor (His-Pro-Asn-Trp-Ser-Lys-Tyr-Iie-Leu-His-Gln-Arg-Gly-Gly-gly-Cys), TNT receptor (Trp-His-Trp), capable of responding to TNT, DNT, RDX explosives real time together, the next thing is the research group that will be published.

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