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Hybridised Single-Phase Cascaded Multilevel Inverter Topology Using Reduced Number of Power Switches

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Abstract: *This paper presents a hybridized single-phase cascaded multilevel inverter topology using reduced number of power switches. The multicarrier, phase disposition pulse width modulation technique is used to generate the switching signals for the power switches. The circuit configuration, mode of operations and the switching functions are given. At a modulation index of 0.8, the desired multilevel inverter's output voltage is obtained. The inverter topologies are subjected to the same values of an R-L load. Logic circuit configuration of the proposed cascaded multilevel inverter is displayed, which generates the firing pulses. The first quarter of the quarter symmetry output voltage waveform is analysed with different displacement angles calculated. Fast Fourier transform analyses of the output voltages of cascaded diode clamped and proposed are displaced under 0.8 modulation index and their respective THD obtained. THD values of 14.38%, 10.32% and 10.43% for cascaded capacitor clamped, diode clamped and proposed are obtained respectively. The proposed configuration with less number of power switches is validated with cascaded diode clamped configuration using simulation approach. Similar results are obtained.*

Index Terms *- Inverter, multicarrier, multilevel, Fast Fourier transform, total harmonic distortion.*

I. INTRODUCTION

Nowadays, Fossil fuel is the major energy supplier of the world economy. This type of energy source has a great advance effect such as global warming which causes serious depletion of ozone layer and air pollution. Therefore, with regard to the worldwide trend of green energy, solar power technology has become one of the most promising energy sources [1]. According to the law of conversion of energy, Sun energy is converted into electrical energy with uncontrolled low d. c. voltage output. Furthermore, an inverter is used to convert direct current into single or poly-phase alternating current. Due to high harmonic content of this conventional inverter a new inverter topology was developed which helps to improve on the problem associated with the conventional type. The staircase waveforms produced from several levels approach the sinusoidal waveform with low harmonic distortion; thus reducing filter requirements [2]. Multilevel inverter configuration is one of the most vital discoveries in power electronics in the recent years. The unique structure of multi-level voltage source inverters allow them to reach high voltages with low harmonics without the use of transformer or series connected synchronized switching devices. As the number of voltage levels increases, the harmonic content of output voltage waveform decreases significantly [3]. Applying this concept, the power conversion is performed with enhanced power quality [4].

Among various multilevel topologies, the most important ones are [5]. Diode Clamped Multilevel Inverter (DCMI) and Flying Capacitor Multilevel Inverter (FCMI) and Cascaded Multilevel Inverter (CMI). The main drawbacks of DCMI topology, with level number higher than three, is the necessity of a capacitor voltage balancing control circuit and the high voltage drop across the clamped diodes. FCMI uses flying capacitors as clamping devices. These configurations have several attractive properties in comparison with DCMI, including the advantages of the transformerless operation and redundant phase leg states that allow the switching stresses to be equally distributed between semiconductors switches [3, 4]. The first, simplest and the most modular topology is CMI [1]. CMI can avoid more clamping diodes or voltage balancing capacitors in the power circuit configuration. It involves series of single phase conventional inverter or hybridised multilevel inverter topologies. Henceforth, the major fault associated with CMI configuration is the need for separated DC sources which are not readily available without the use of transformers. In some specific applications such as photovoltaic systems, electric vehicle motor drive, separate dc sources exists and can be used in the CMI configuration.

For the modulation of multilevel inverters, carrier-based modulation schemes are normally used, largely divided into two categories: phase-shifted carrier pulse width modulation and level-shifted width modulation [6]. Fig. 1 shows the multilevel converter modulation methods. The modulation control schemes for the multilevel can be divided into two categories, fundamental switching frequency and high switching frequency PWM such as carrier-based PWM , selective harmonic elimination and multilevel space vector PWM Multilevel SPWM needs multiple carriers [7]. One of the simplest modulation strategies for CMI is phase shifted carrier modulation technique where the n carriers of the full bridge cascaded inverters are phase shifted by 180/n degrees [1]. This modulation technique is utilized due to its simplicity. It is observed that this method of modulation is not suitable for all resistive-induction loads and it is also associated with high harmonic contents. Due to shortcomings of this modulation technique, in this paper, sinusoidal pulse width modulation (PWM) technique is implemented.

In this paper, a hybridised single-phase cascaded multilevel inverter topology using reduced number of power switches is proposed. The power circuit configuration of (Diode clamped Multilevel cascaded inverter) DCMCI and proposed hybridized cascaded MI are presented in Section II. The Pulse width modulation (PWM) control method is introduced in Section III. The simulation results for validating the improvements of the proposed inverter topology are in Section IV. In Section V conclusion is presented.

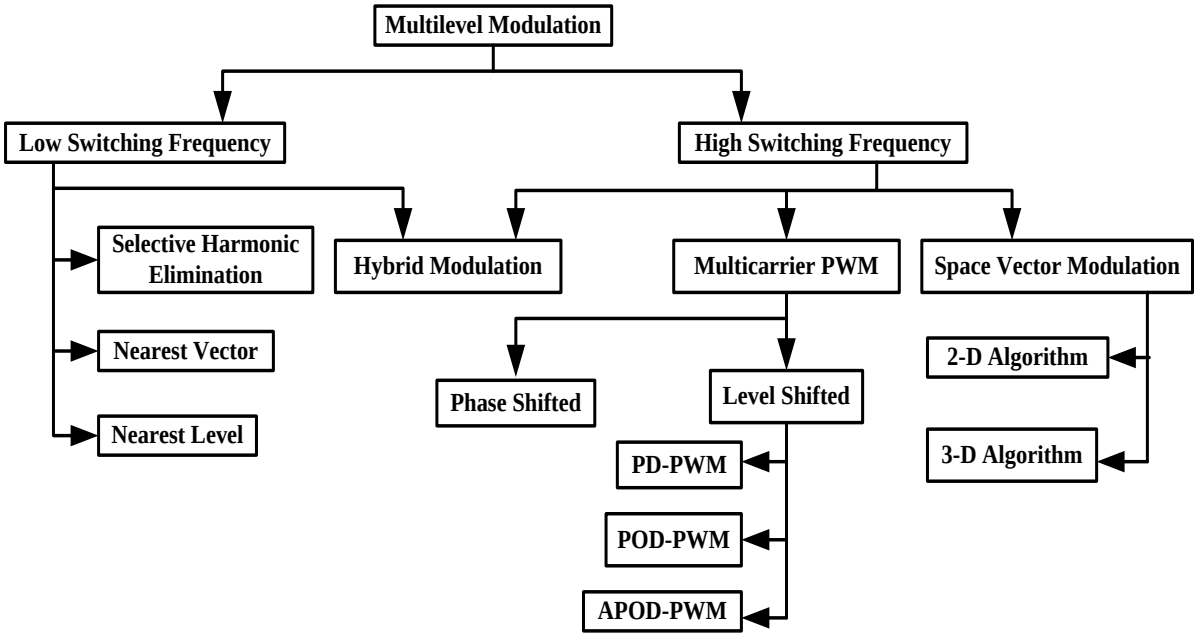

Fig. 1 Multilevel converter modulation methods

II. POWER CIRCUIT CONFIGURATION OF THREE-LEVEL INVERTER TOPOLOGIES.

The Fig. 2 below shows, a power circuit configuration of a Diode clamped multilevel cascaded inverter topology. Each of the cells comprises of a single-phase three-level diode clamped inverter with one dc source and two voltage divided capacitors. Also, each of the cells comprises of eight power switches with anti-parallel diodes and four clamping diodes. Furthermore, each of the cells contains four upper switches and four lower switches. Thus, the power switches can be arranged in the form of four power switches per leg voltage.

The proposed hybridized single-phase cascaded multilevel inverter topology is shown in Fig. 3. The inverter is comprised of two cells of single-phase conventional H-bridge, one bidirectional power switch, two capacitors which serve as dc voltage divider. The bidirectional circuit is connected to the centre tap of the capacitor voltage divider. In Figs. 1 and 2, the proper switching of the inverter can generate the following output-voltage levels: $2V_{dc}$, $3V_{dc}/_2$, $V_{dc}/_2$,0, $-V_{dc}/_2$, $-3V_{dc}/_2$, $-2V_{dc}$. The addition of switches S_A and S_B must be properly switched considering the direction of the flow of the load current [4]. The switching pattern adopted by DCMCI and proposed inverter topologies are shown in Figs. 6 and 7 respectively. Thus, Table 1 shows the switching combinations that generated the output voltage level aforementioned above.

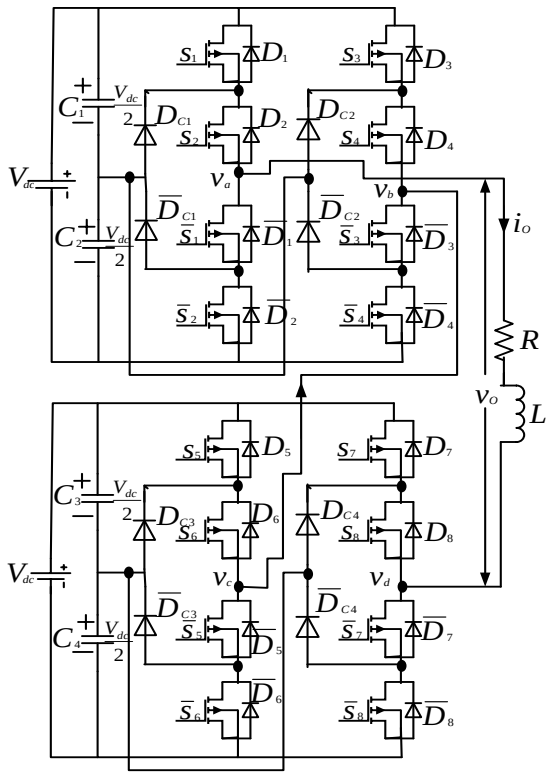

Fig. 2 Configuration of the ideal diode clamped single-phase cascaded multilevel Inverter.

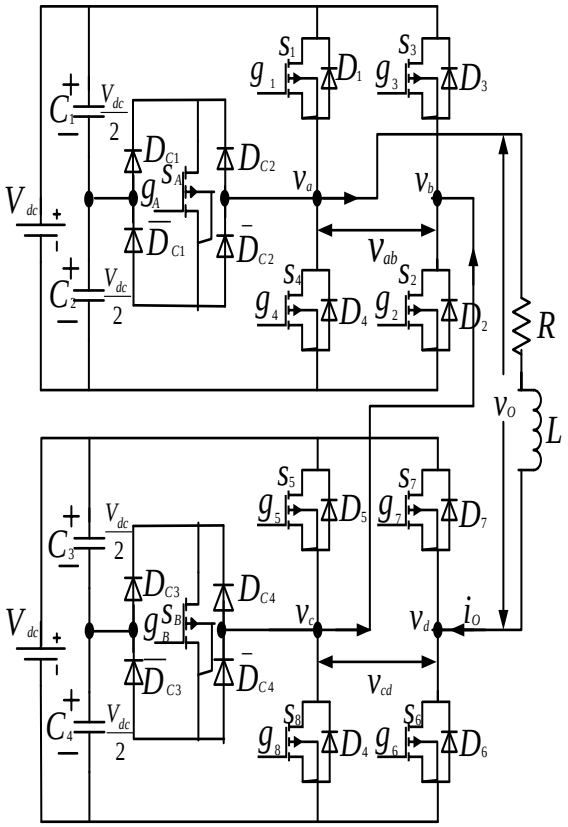

Fig. 3 Configuration of the proposed single-phase cascaded multilevel inverter.

Table 1 Output voltage according to the switches on/off (1/0) conditions

S/N	s_1	s_2	s_3	s_4	s_5	s_6	s_7	s_8	s_A	s_B	v_a	v_b	v_c	v_d	v_{ab}	v_{cd}	v_o
1	0	1	0	0	0	1	0	1	1	0	$\frac{V_{dc}}{2}$	0	0	0	$\frac{V_{dc}}{2}$	0	$\frac{V_{dc}}{2}$
2	1	1	0	0	0	1	0	1	0	0	V_{dc}	0	0	0	V_{dc}	0	V_{dc}
3	1	1	0	0	0	1	0	0	0	1	V_{dc}	0	$\frac{V_{dc}}{2}$	0	V_{dc}	$\frac{V_{dc}}{2}$	$\frac{3V_{dc}}{2}$
4	1	1	0	0	1	1	0	0	0	0	V_{dc}	0	V_{dc}	0	V_{dc}	V_{dc}	$2V_{dc}$
5	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0
6	1	0	1	0	1	0	1	0	0	0	V_{dc}	V_{dc}	V_{dc}	V_{dc}	0	0	0
7	0	0	1	0	1	0	1	0	1	0	$\frac{V_{dc}}{2}$	V_{dc}	V_{dc}	V_{dc}	$\frac{-V_{dc}}{2}$	0	$\frac{-V_{dc}}{2}$
8	0	0	1	1	1	0	1	0	0	0	0	V_{dc}	V_{dc}	V_{dc}	$-V_{dc}$	0	$-V_{dc}$
9	0	0	1	1	0	0	1	0	0	1	0	V_{dc}	$\frac{V_{dc}}{2}$	V_{dc}	$-V_{dc}$	$\frac{-V_{dc}}{2}$	$\frac{-3V_{dc}}{2}$
10	0	0	1	1	0	0	1	1	0	0	0	V_{dc}	0	V_{dc}	$-V_{dc}$	$-V_{dc}$	$-2V_{dc}$

III. PWM MODULATION

Multilevel inverters using pulse-width modulation are being increasingly preferred for high-power applications. The advantages of multilevel inverters are their ability to generate voltage waveforms with lower harmonics, without resorting to high-frequency PWM switching [8]. Multicarrier phase disposition PWM control scheme is employed in the generation of the gating signals. Basic principle of the proposed switching strategy is to generate gate signals by comparing the rectified sinusoidal modulating/reference signal, at fundamental frequency, with four triangular carrier waves having higher switching frequency and in-phase, but different offset voltages [4].

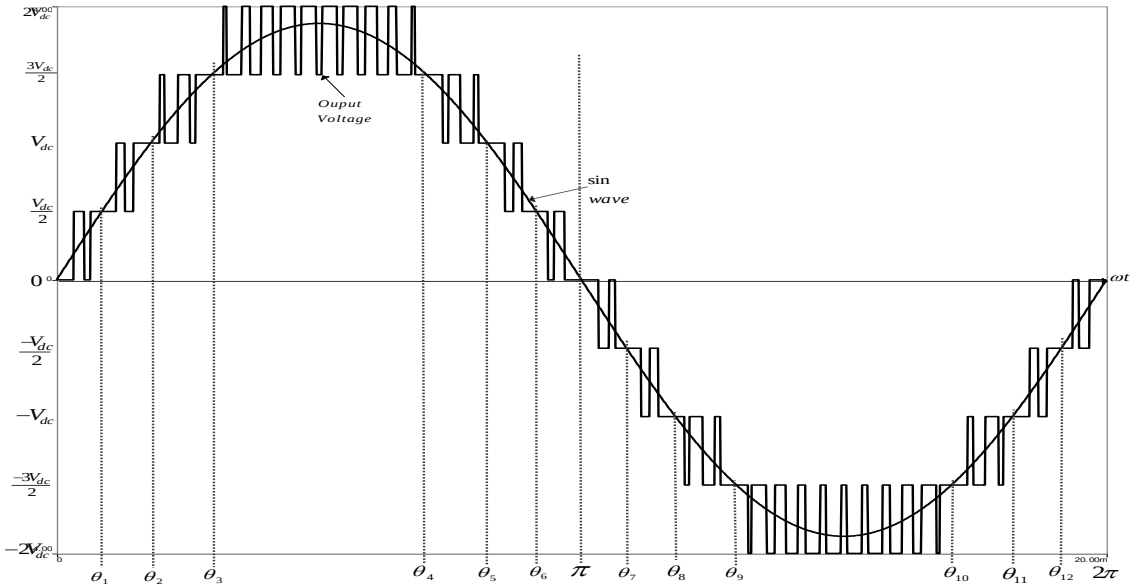

Fig. 4 Inverter Output Voltage and switching angles.

For one period of the expected output voltage and reference voltage is given in Fig. 4. This voltage plot profile shows how much our expected output voltage waveform differs from the reference waveform. The two inverter topologies operate through eight modes. Therefore (1) is generated from Fig. 4 and also showcases the eight modes operation.

$$f(\omega t) = \begin{cases} 0 \text{ and } \frac{V_{dc}}{2},\ 0 < \omega t < \theta_1, \text{mode } 1 \\ \frac{V_{dc}}{2} \text{ and } V_{dc},\ \theta_1 < \omega t \geq \theta_2, \text{mode } 2 \\ V_{dc} \text{ and } \frac{3V_{dc}}{2},\ \theta_2 < \omega t < \theta_3, \text{mode } 3 \\ \frac{3V_{dc}}{2} \text{ and } 2V_{dc},\ \theta_3 < \omega t < \theta_4, \text{mode } 4 \\ \frac{3V_{dc}}{2} \text{ and } V_{dc},\ \theta_4 < \omega t < \theta_5, \text{mode } 3 \\ V_{dc} \text{ and } \frac{V_{dc}}{2},\ \theta_5 < \omega t < \theta_6, \text{mode } 2 \\ \frac{V_{dc}}{2} \text{ and } 0,\ \theta_6 < \omega t < \pi, mode\ 1 \\ 0 \text{ and } \frac{-V_{dc}}{2},\ \pi < \omega t < \theta_7, \text{mode } 5 \\ \frac{-V_{dc}}{2} \text{ and } -V_{dc},\ \theta_7 < \omega t \geq \theta_8, \text{mode } 6 \\ -V_{dc} \text{ and } \frac{-3V_{dc}}{2},\ \theta_8 < \omega t < \theta_9, \text{mode } 7 \\ \frac{-3V_{dc}}{2} \text{ and } -2V_{dc},\ \theta_9 < \omega t < \theta_{10}, \text{mode } 8 \\ \frac{-3V_{dc}}{2} \text{ and } -V_{dc},\ \theta_{10} < \omega t < \theta_{11}, \text{mode } 7 \\ -V_{dc} \text{ and } \frac{-V_{dc}}{2},\ \theta_{11} < \omega t < \theta_{12}, \text{mode } 6 \\ \frac{-V_{dc}}{2} \text{ and } 0,\ \theta_{12} < \omega t < 2\pi, mode\ 5 \end{cases} \quad (1)$$

The phase angle depends on modulation index M_a. Theoretically, for a single reference signal reference signal carrier signal, the modulation index is defined to be

$$M_a = \frac{A_m}{A_c} \quad (2)$$

While for a single-reference signal and dual carrier signal, the modulation index is defined to be [9]

$$M_a = \frac{A_m}{2A_c} \quad (3)$$

Generally, the expression of moduation index is given as [2]

$$M_a = \frac{A_m}{A_c(k-1)} \quad (4)$$

Where A_c is the peak-to-peak value of the triangular carrier signals, A_m is the apex value of the rectified sinusoidal reference and k is the number of output voltage level synthesized per half-cycle; in this case, k=5.

When modulation index is less than 0.25, the phase angle displacement is

$$\theta_1 = \theta_2 = \theta_3 = \theta_4 = \theta_5 = \theta_6 = \frac{\pi}{2} \quad (5)$$

$$\theta_7 = \theta_8 = \theta_9 = \theta_{10} = \theta_{11} = \theta_{12} = \frac{3\pi}{2} \quad (6)$$

Furthermore, when the modulation index is more than 0.25 and less than or equal to 0.50, the phase angle displacement is determined by

$$\theta_1 = sin^{-1}\left(\frac{A_c}{A_m}\right) \quad (7)$$

$$\theta_2 = \theta_3 = \theta_4 = \theta_5 = \frac{\pi}{2} \quad (8)$$

$$\theta_6 = \pi - \theta_1 \quad (9)$$

$$\theta_7 = \pi + \theta_1 \quad (10)$$

$$\theta_8 = \theta_9 = \theta_{10} = \theta_{11} = \frac{3\pi}{2} \quad (11)$$

$$\theta_{12} = 2\pi - \theta_1 \quad (12)$$

Moreover, when the modulation index is more than 0.50 and less than or equal to 0.75, the phase angle displacement is determined by

$$\theta_1 = sin^{-1}\left(\frac{A_c}{A_m}\right) \quad (13)$$

$$\theta_2 = sin^{-1}\left(\frac{2A_c}{A_m}\right) \quad (14)$$

$$\theta_3 = \theta_4 = \frac{\pi}{2} \quad (15)$$

$$\theta_5 = \pi - \theta_2 \quad (16)$$

$$\theta_6 = \theta_7 = \pi - \theta_1 \quad (17)$$

$$\theta_8 = \pi + \theta_2 \quad (18)$$

$$\theta_9 = \theta_{10} = \frac{3\pi}{2} \quad (19)$$

$$\theta_{11} = 2\pi - \theta_2 \quad (20)$$

$$\theta_{12} = 2\pi - \theta_1 \quad (21)$$

Finally, when the modulation index is greater than 0.750, the phase angle displacement is determined by

$$\theta_1 = sin^{-1}\left(\frac{A_c}{A_m}\right) \quad (22)$$

$$\theta_2 = sin^{-1}\left(\frac{2A_c}{A_m}\right) \quad (23)$$

$$\theta_3 = sin^{-1}\left(\frac{3A_c}{A_m}\right) \quad (24)$$

$$\theta_4 = \pi - \theta_3 \quad (25)$$

$$\theta_5 = \pi - \theta_2 \quad (26)$$

$$\theta_6 = \pi - \theta_1 \quad (27)$$

$$\theta_7 = \pi + \theta_1 \quad (28)$$

$$\theta_8 = \pi + \theta_2 \quad (29)$$

$$\theta_9 = \pi + \theta_3 \quad (30)$$

$$\theta_{10} = 2\pi - \theta_3 \quad (31)$$

$$\theta_{11} = 2\pi - \theta_2 \quad (32)$$

$$\theta_{12} = 2\pi - \theta_1 \quad (33)$$

The frequency modulation index [10] is given as

$$M_f = \frac{f_c}{f_m} \quad (34)$$

Where, f_c is the frequency of the carrier wave and f_m is the frequency of the sinusoidal wave.

For M_a equal to or less than, 0.25, only the lower triangular carrier wave (Tri) is compared with the rectified reference wave (Sin). The inverter's behaviour is similar to a conventional full-bridge. If M_a is greater than 0.25 and less than 0.50, two triangular carrier signals, Tri and Tri1, are compared with the rectified reference wave. The inverter's output voltage behavior is similar to a fundamental multilevel inverter. Furthermore, when M_a is

greater than 0.50 and less than 0.75, three triangular carrier signals, Tri, Tri1 and Tri2, are compared with the rectified reference wave (Sin). Four levels of output voltage are synthesized on positive half cycle. Finally, when M_a is set to be greater than 0.75 for nine levels of output voltage to be produced in this work. In this case, all the four triangular carrier signals, Tri-Tri3 have to be compared with the reference to generate switching signals for the power switches [4].

In Fig. 5, it can be seen that eight switching signals: g_1, $\bar{g}_1$, g_2, $\bar{g}_2$, g_5, $\bar{g}_5$, g_6, and $\bar{g}_6$ are operating at the rate of carrier signals' frequency; whereas eight other switching signals: g_3, $\bar{g}_3$, g_4, $\bar{g}_4$, g_7, $\bar{g}_7$, g_8, and $\bar{g}_8$ are operating at the fundament frequency. In Fig. 6, it can be seen that six switching signals: g_1, g_4, g_5, g_8, g_A and g_B, are operating at the rate of carrier signals' frequency (f_c); whereas four other switching signals: g_2, g_3, g_6 and g_7, are operating at the fundament frequency (f_m). In Fig. 7 shows how the overall firing circuit signals of the proposed hybridised single-phase cascaded multilevel inverter are generated.

Fig. 7(A) depicts how rectified reference wave (Sin) is been generated from the fundamental reference sine wave (50Hz) by passing the signal through rectifier circuit. Signals g_2 and g_6 are generated by comparing the reference sine wave with zero potential. Consequently, inverting g_2 and g_6 yield g_3 and g_7. Signal g_1 is generated by combination of Op-Amp comparators, AND and OR gates. Also, the carrier signals Tri1, Tri2 and Tri3 are generated from fundamental carrier triangular wave operating at 2KHz with the aid of level-shifter circuits.

In Fig. 7(B), the switching signals of g_4, g_5 and g_8 are generated with the help of signal generated in Fig. 7(A). In the same way, switching signals of g_A and g_B are generated with the help of Figs. 7(C) and 7(D) respectively. For easy troubleshooting and to avoid complexity in the circuit configurations in Fig. 7, it is embedded in a subsystem using Matlab-Simulink with two inputs and eight outputs as the case maybe.

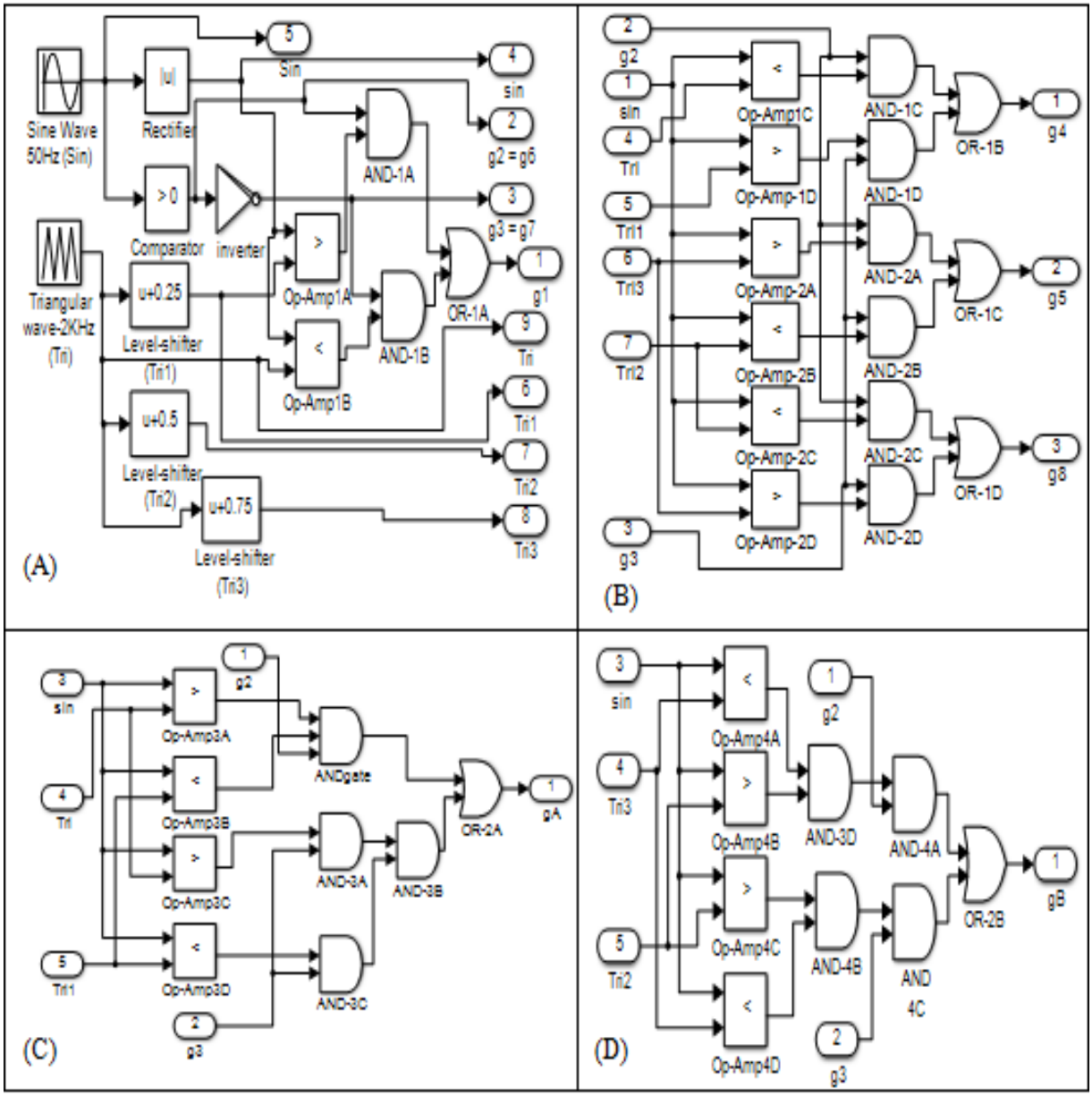

Fig. 7 Logic control circuit for the proposed multilevel inverter topology.

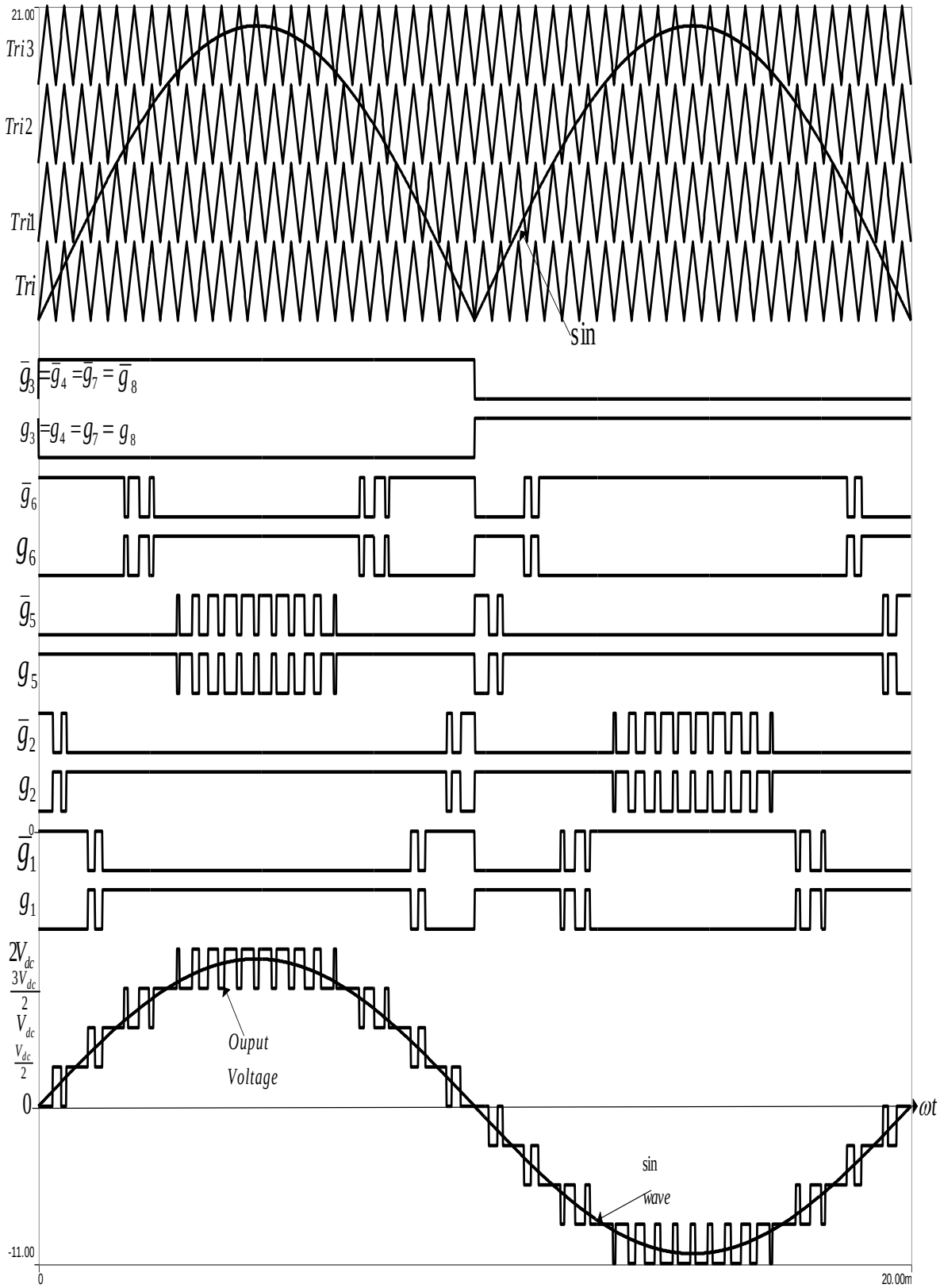

Fig. 5 Switching patterns of the diode clamped single-phase, five-level cascaded multilevel inverter.

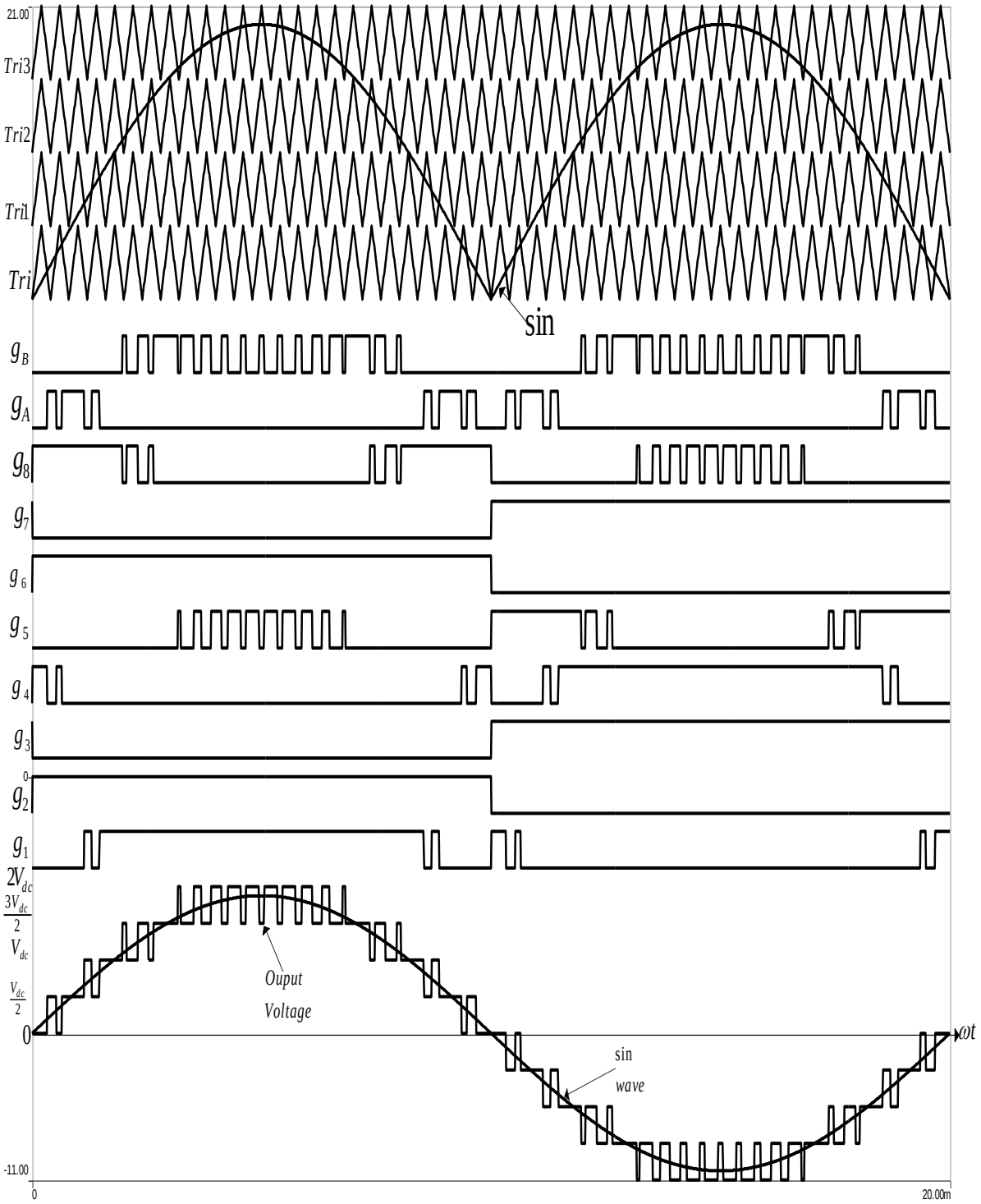

Fig. 6 Switching patterns of the proposed single-phase, five-level hybridised cascaded multilevel inverter.

The output voltage control of inverters requires varying both the number of pulses per half-cycle and the pulse widths generated by modulating techniques. Fig. 8 shows the first quarter of the quarter-wave symmetric waveform with twenty one phase displacement angles. The output voltage contains odd harmonics over a frequency spectrum. Assuming $a_0 = a_n = 0$, therefore (35) can be rewritten as (40).

The Fourier series of the periodic function of the output voltage can be expressed as

$$V_o(\omega t) = a_0 + \sum_{n=1}^{\infty} (a_n \cos n\omega t + b_n \sin n\omega t) \qquad (35)$$

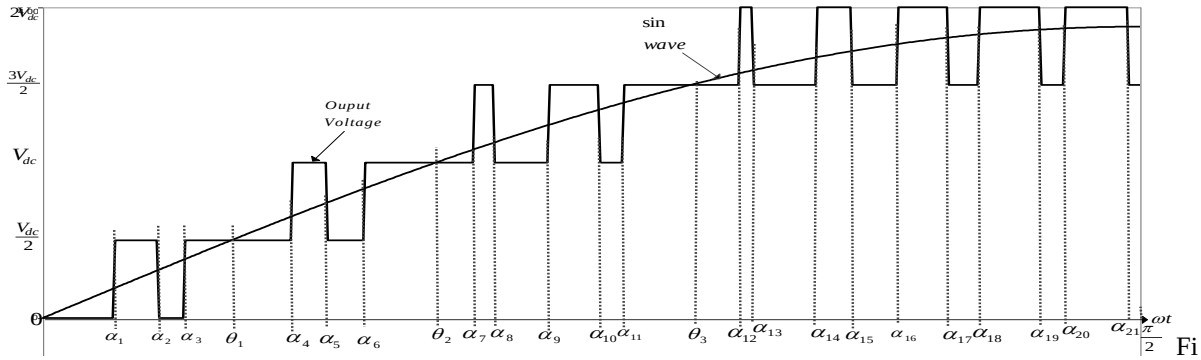

Fig. 8 The first quarter of the quarter-wave symmetric waveform.

At the interval of 0 and θ_1, we have

$$f_1(\omega t) = \begin{Bmatrix} \frac{V_{dc}}{2},\ \alpha_1 < \omega t < \alpha_2 \\ \frac{V_{dc}}{2},\ \alpha_3 < \omega t < \theta_1 \end{Bmatrix} \quad (36)$$

At the interval of θ_1 and θ_2, we have

$$f_2(\omega t) = \begin{Bmatrix} \frac{V_{dc}}{2},\ \theta_1 < \omega t < \alpha_4 \\ V_{dc},\ \alpha_4 < \omega t < \alpha_5 \\ \frac{V_{dc}}{2},\ \alpha_5 < \omega t < \alpha_6 \\ V_{dc},\ \alpha_6 < \omega t < \theta_2 \end{Bmatrix} \quad (37)$$

At the interval of θ_2 and θ_3, we have

$$f_3(\omega t) = \begin{Bmatrix} V_{dc},\ \theta_2 < \omega t < \alpha_7 \\ \frac{3V_{dc}}{2},\ \alpha_7 < \omega t < \alpha_8 \\ V_{dc},\ \alpha_8 < \omega t < \alpha_9 \\ \frac{3V_{dc}}{2},\ \alpha_9 < \omega t < \alpha_{10} \\ V_{dc},\ \alpha_{10} < \omega t < \alpha_{11} \\ \frac{3V_{dc}}{2},\ \alpha_{11} < \omega t < \theta_3 \end{Bmatrix} \quad (38)$$

At the interval of θ_3 and $\frac{\pi}{2}$, we have

$$f_4(\omega t) = \begin{Bmatrix} \frac{3V_{dc}}{2},\ \theta_3 < \omega t < \alpha_{12} \\ 2V_{dc},\ \alpha_{12} < \omega t < \alpha_{13} \\ \frac{3V_{dc}}{2},\ \alpha_{13} < \omega t < \alpha_{14} \\ 2V_{dc},\ \alpha_{14} < \omega t < \alpha_{15} \\ \frac{3V_{dc}}{2},\ \alpha_{15} < \omega t < \alpha_{16} \\ 2V_{dc},\ \alpha_{16} < \omega t < \alpha_{17} \\ \frac{3V_{dc}}{2},\ \alpha_{17} < \omega t < \alpha_{18} \\ 2V_{dc},\ \alpha_{18} < \omega t < \alpha_{19} \\ \frac{3V_{dc}}{2},\ \alpha_{19} < \omega t < \alpha_{20} \\ 2V_{dc},\ \alpha_{20} < \omega t < \alpha_{21} \\ \frac{3V_{dc}}{2},\ \alpha_{21} < \omega t < \frac{\pi}{2} \end{Bmatrix} \quad (39)$$

$$V_o(\omega t) = \sum_{n=1,3,5}^{\infty} b_n \sin n\omega t \quad (40)$$

Where,

$$b_n = \frac{4V_{dc}}{n\pi}\left[\int_0^{\theta_1} f_1(\omega t)\sin(n\omega t)d(\omega t) + \int_{\theta_1}^{\theta_2} f_2(\omega t)\sin(n\omega t)d(\omega t) + \int_{\theta_2}^{\theta_3} f_3(\omega t)\sin(n\omega t)d(\omega t) + \int_{\theta_3}^{\frac{\pi}{2}} f_4(\omega t)\sin(n\omega t)\,d(\omega t)\right]$$

(41)

Where $\alpha_1 < \alpha_2 < \alpha_3 < \alpha_4 < \alpha_5 < \alpha_6 < \alpha_7 < \alpha_8 < \alpha_9 < \alpha_{10} < \alpha_{11} < \alpha_{12} < \alpha_{13} < \alpha_{14} < \alpha_{15} < \alpha_{16} < \alpha_{17} < \alpha_{18} < \alpha_{19} < \alpha_{20} < \alpha_{21} < \frac{\pi}{2}$.

Therefore, the coefficient b_n is given by

$$b_n = \frac{2V_{dc}}{n\pi}\left[\cos(n\alpha_1) - \cos(n\alpha_2) + \cos(n\alpha_3) + \cos(n\alpha_4) - \cos(n\alpha_5) + \cos(n\alpha_6) + \cos(n\alpha_7) - \cos(n\alpha_8) + \cos(n\alpha_9) - \cos(n\alpha_{10}) + \cos n\alpha_{11} + \cos(n\alpha_{12}) - \cos(n\alpha_{13}) + \cos(n\alpha_{14}) - \cos(n\alpha_{15}) + \cos(n\alpha_{16}) - \cos(n\alpha_{17}) + \cos(n\alpha_{18}) - \cos(n\alpha_{19}) + \cos(n\alpha_{20}) - \cos(n\alpha_{21}) - \frac{3}{2}\cos\left(\frac{n\pi}{2}\right)\right]$$

(42)

The Higher harmonic contents would be eliminated if

$$b_3 = b_5 = b_7 = b_9 = b_{11} = b_{13} = b_{15} = b_{17} = b_{19} = b_{21} = b_{23} = b_{25} = b_{27} = b_{29} = b_{31} = b_{33} = b_{35} = b_{37} = b_{39} = b_{41} = b_{43} = 0. \quad (43)$$

Solving these equations in equation (43) by iterations using Matlab program, we get $\alpha_1 = 5.3606°$, $\alpha_2 = 8.0233°$, $\alpha_3 = 10.6585°$, $\alpha_4 = 21.4047°$, $\alpha_5 = 24.0745°$, $\alpha_6 = 26.6632°$, $\alpha_7 = 37.9141°$, $\alpha_8 = 40.1660°$, $\alpha_9 = 43.8252°$, $\alpha_{10} = 48.3582°$, $\alpha_{11} = 50.3648°$, $\alpha_{12} = 50.5074°$, $\alpha_{13} = 50.8514°$, $\alpha_{14} = 62.6155°$, $\alpha_{15} = 64.2135°$, $\alpha_{16} = 69.4697°$, $\alpha_{17} = 72.2154°$, $\alpha_{18} = 76.6397°$, $\alpha_{19} = 80.2819°$, $\alpha_{20} = 84.0820°$, and $\alpha_{21} = 88.1564°$

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IV. SIMULATION RESULTS

In other to see the performance of the conventional 5-level cascaded diode clamped and proposed inverter topologies, a MATLAB-SIMULINK software simulation was used. The PWM switching patterns generated aforementioned are used to drive the power switches ($s_1 - s_8$, s_A and s_B). Dc-source voltage in each cell is 100V, and dividing capacitor value of 3900µF by 50V. An R-L load is connected at the output terminals of the inverter; whose values are 50Ω and 0.05mH, respectively. Figs. 9[a] and 9[b] show the cascaded diode clamped output V_{ab} and V_{cd} respectively for two cycles.Thus, Figs. 9[c] and 9[d] depict the inverter output voltage and current respectively. For a modulation index of 0.8, a THD 10.32% is obtained as shown in Fig.10.

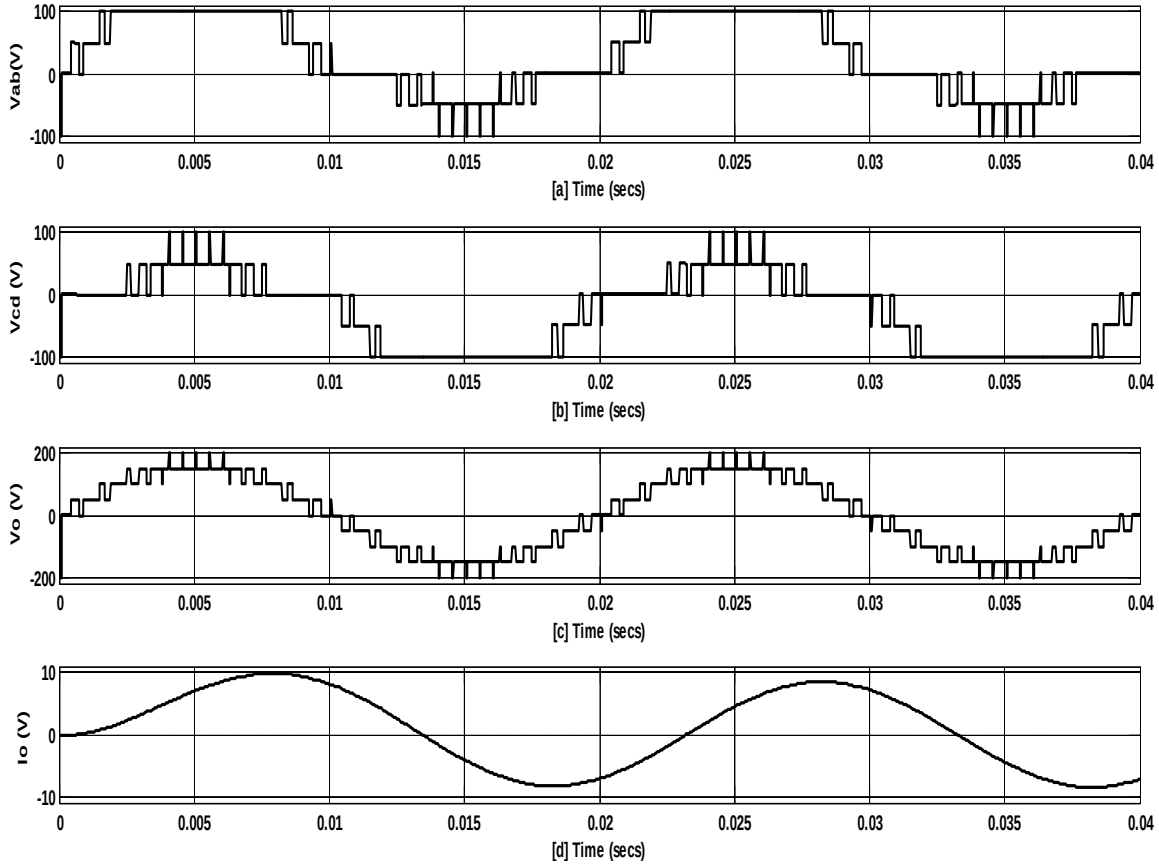

Fig. 9 Simulation result of voltage and current of cascaded diode clamped multilevel inverter.

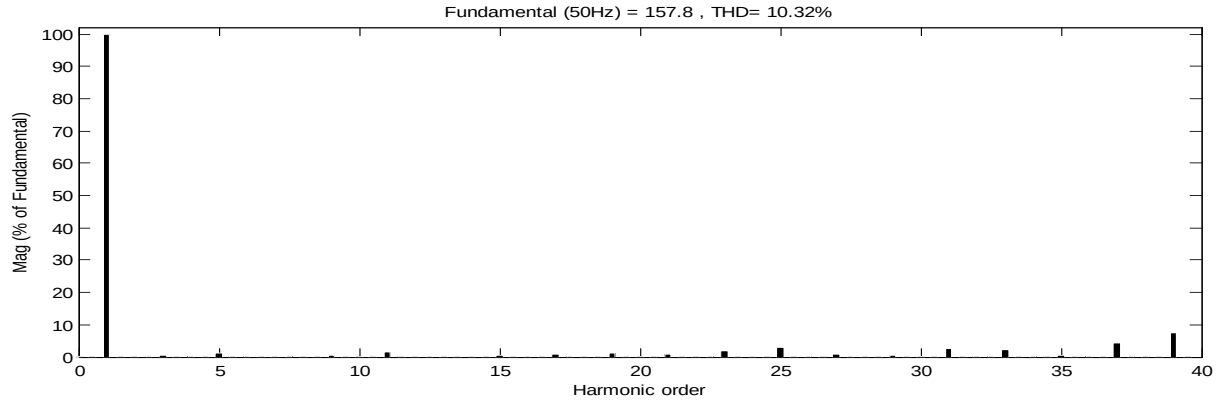

Fig. 10 Harmonic profile of the inverter output voltage for cascaded diode clamped inverter.

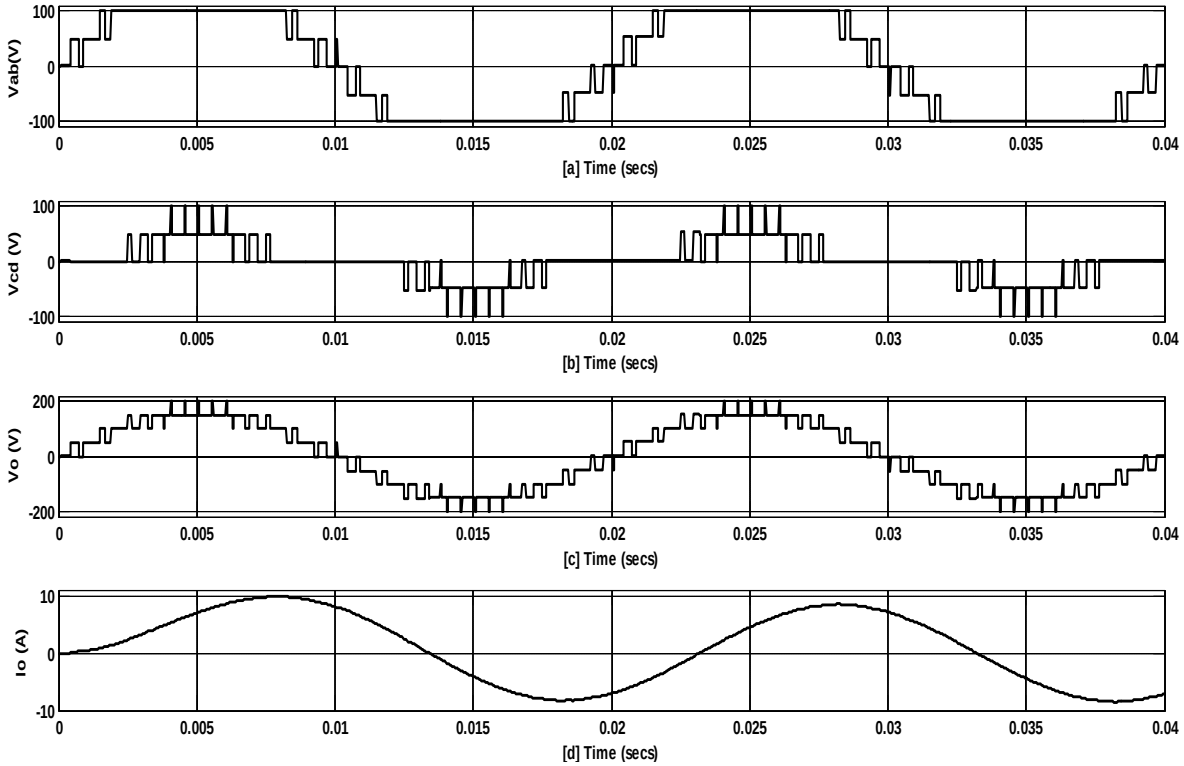

Fig. 11 Simulation result of voltages and current of cascaded proposed multilevel inverter.

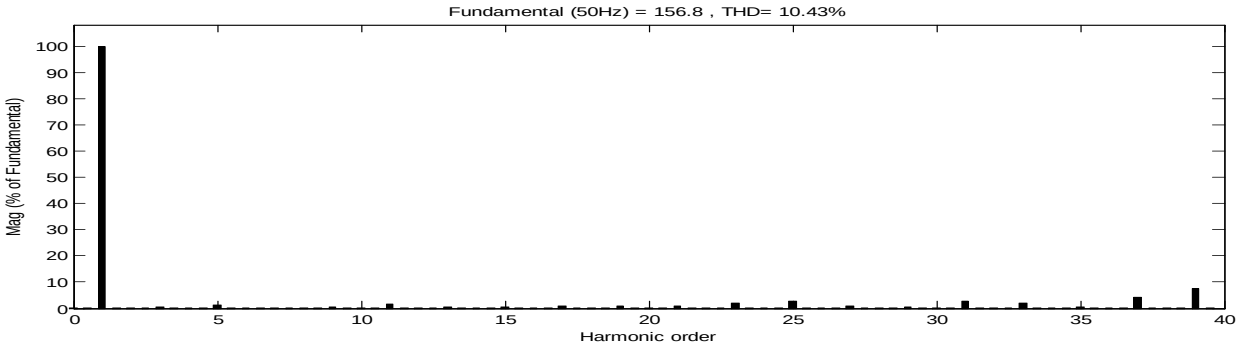

Fig. 12 Harmonic profile of the inverter output voltage for cascaded proposed inverter.

In Figs. 11[a] and 11[b] show the cascaded diode clamped output V_{ab} and V_{cd} respectively for two cycles. Thus, Figs. 11[c] and 11[d] depict the inverter output voltage and current respectively. For a modulation index of 0.8, a THD 10.43% is obtained as shown in Fig.12. Table 2 depicts total harmonic distortion comparison between the different cascaded H-bridge and proposed power circuit configurations.

Table 2 Comparison of THD

Cascaded H-bridge Power Circuit Topology	Line-Line Voltage THD (%)
5-Level FLC	14.38
5-Level NPC	10.32
5-Level Proposed	10.43

V. CONCLUSION

This paper has proposed a hybridised single-phase cascaded multilevel inverter topology using reduced number of power switches. The operational principles, modulation technique and switching functions has been analysed in detail. The desired output voltage form has been obtained at modulation index of 0.8 and frequency index of 40. Also, the per cell output voltage has been obtained through simulation. The proposed topology has a

THD of 10.43% in the output voltage waveform. The modulation approach and the proposed power circuit configuration adopted in this work will contribute immensely in reducing the power inverter cost and weight.

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