

CMOS BASED CURRENT FEEDBACK OP-AMP WITH IMPROVED BANDWIDTH

Akshay Dubey

Research Scholar, Electronics Engineering department,
Institute of Engineering and Technology, Lucknow, India.

ABSTRACT : A current mode feedback operational amplifier designed using a complimentary MOS circuit technology has been discussed in this paper. A class AB amplifier has been used in the design and the design results in improvement of values of number of parameter when compared to the previously reported architecture. The circuit is designed using 0.35 μ m technology. Bandwidth of the presented architecture was obtained, that was always greater than 50MHz. On the other hand, bandwidth in case of previously reported circuit was coming out to be always more than 2MHz. Thus in our proposed circuit, there is a considerable improvement in the bandwidth of the circuit. Also the Slew rate, which was improved from 5.2V/ μ sec to 8.1V/ μ sec. Settling time of the proposed circuit has been reduced to 134 nsec which was of order of 212 nsec in case of the previous design.

Keywords - Amplifiers, CMOS, current-feedback operational amplifiers (CFOAs), Slew Rate.

I. INTRODUCTION

An operational amplifier (op amp) is a device whose output is the multiplication of its internal gain and the differential voltage applied to its input terminals. It was initially used for analog computation and instrumentation. It wasn't until the mid 1960's and the invention of the integrated circuit (IC) that the op amp's full versatility was realized.

Earlier, an ideal op amp has been classified as a differential input, single ended output amplifier with infinite gain, infinite input resistance, and zero output resistance. But after the invention of the first IC, manufacturers of op amps have almost got very closer to approximate these characteristics of an ideal op amp. There are continuous researches going all over the globe to find the ways to increase the input impedance, lower the output impedance, offset currents and voltages and noise. Simultaneously, researchers have been trying to push the bandwidths of the devices higher, and lower the settling-time characteristics. These characteristics are very important, specially in applications such as high speed digital to analog conversion (DAC) buffers, sample and hold (S-H) circuits, switching applications and video and IF drivers.

In spite of all electronic systems prominently being dominated by digital circuits and systems, the analog circuits have neither become obsolete nor avoidable. In fact, analog circuits and techniques continue to be indispensable and unavoidable in many areas since all real life signals are analog in nature [8]. Also many basic functions such as amplification, rectification, continuous time filtering, analog to digital conversion and digital to analog conversion etc. need analog circuits and techniques. Therefore analog circuits act as a bridge between the real world and digital systems. Current feedback operational amplifiers (CFOAs) are the modified version of conventional voltage op-amps and are used in number of applications [1]–[4] for their inherent advantages over conventional op-amps, which are generally expressed in terms of high-speed properties [5], [6]. Also, the (inverting) closed-loop bandwidth of operational amplifier have becomes independent of the closed loop gain, provided, the feedback resistance is kept constant. Besides, the input (output) stage of current feedback op-amp are the voltage buffer that can be easily implemented through class-AB topologies. This enable us achieving a reasonably high slew rate values.

In this paper, we will discuss the implementation of two CFOA architectures. The former was originally proposed by one of the authors in [7], is based on a low-voltage alternative and is modified version of the architecture that was presented in [8] which was based on a well-known class AB differential amplifier stage

with high drive capability. The class AB differential amplifiers are here utilized in unity feedback, and thus allowing us to achieve high slew rate and relatively low input and output resistances. This property also enables a large variation of the closed-loop gain, while maintaining constant the bandwidth. Both the circuit topologies are described in Sections 2 and 3, respectively. Simulations and experimental measurements are given in Section 4. Conclusions are summarized in Section 5.

II. EXISTING ARCHITECTURE

In the architecture presented in [8], the problem of high voltage requirement have been solved by adopting a class-AB unity-gain buffer ,and thus the new architecture require low-voltage supply. The resulting simplified schematic of the low-voltage CFOA is depicted in Fig. 1. M1-M13 form the first unity-gain closed-loop voltage buffer. The input current at the inverting terminal is conveyed to the high impedance node at the drain of M22-M23. Transistors M1b-M13b implement the output buffer. The minimum supply voltage is now reduced to $V_{GS} + 3V_{DS, SAT}$ (path formed by M9b-M1b-M23-M24) and the maximum input swing is $V_{GS} + 3V_{DS, SAT}$ from $V_{DD} - V_{SS} - V_{GS} - 2V_{DS, SAT}$ that was derived in [8].

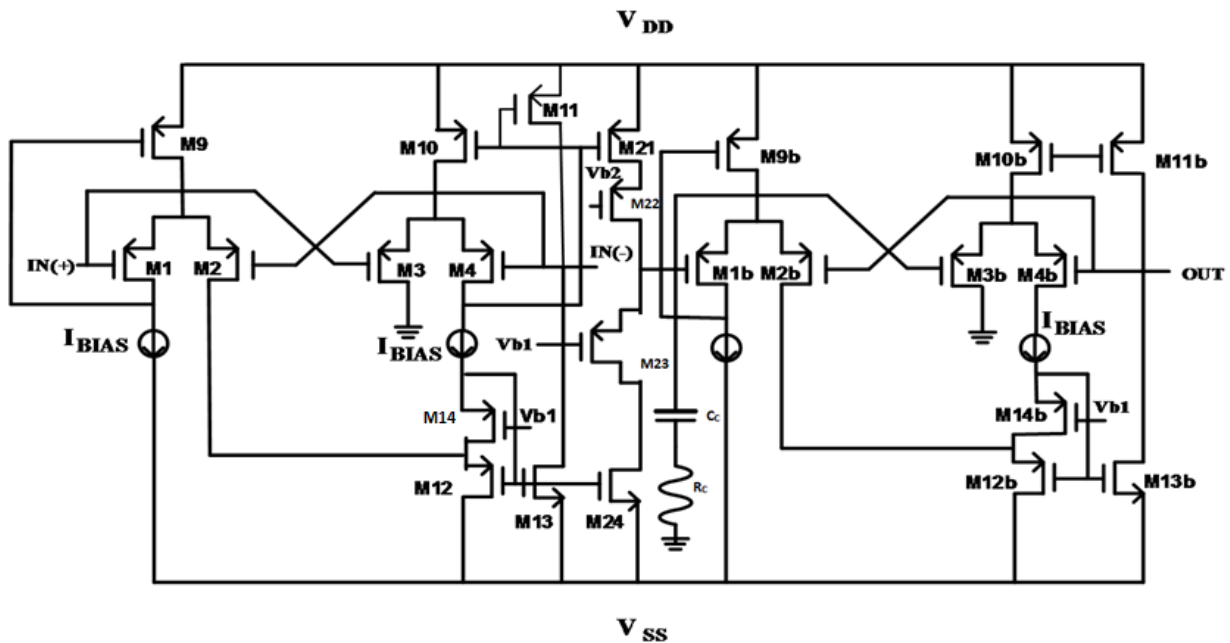


Figure 1. Existing Architecture.

III. PROPOSED ARCHITECTURE WITH IMPROVED BANDWIDTH.

In the circuit presented in fig 3, M1-M13 form the first unity-gain closed-loop voltage buffer. The input current at the inverting terminal is conveyed to the high impedance node at the drain of M22-M23. Transistors M1b-M13b implement the output buffer. In the circuit shown in fig 1, the transistor such as M14, M14b, M11, M22 and M23 is intended to provide stability to the circuit and they are not performing any such special function. Since all the MOS are operating in saturation region and if we are in a position to sacrifice the stability of the circuit to some extent, in order to achieve some fruitful results such as improvement in various parameter, then we can propose a circuit that is shown in fig 3.

In the proposed circuit shown in fig 3, MOSFET M11, M14, M14b, M22 and M23 has been removed and the resultant circuit results were studied on a Tanner EDA tool. By doing so, we have achieved improvement in the verious parameter.

Dominant-pole frequency compensation is obtained through capacitor C_C whereas resistor R_C introduces, as usual, a negativezero. The input resistance, (at the inverting input terminal) and the output resistance are expressed by:

$$r_{in}^- = \frac{1}{g_{m4}} \parallel \frac{1}{g_{m8}} \tag{1}$$

$$r_{out} = \frac{1}{g_{m4b}} \parallel \frac{1}{g_{m8b}} \tag{2}$$

The gain bandwidth product is given by:

$$\omega_{GBW} = \frac{1}{(r_{in}^- + r_{out})C_c} \tag{3}$$

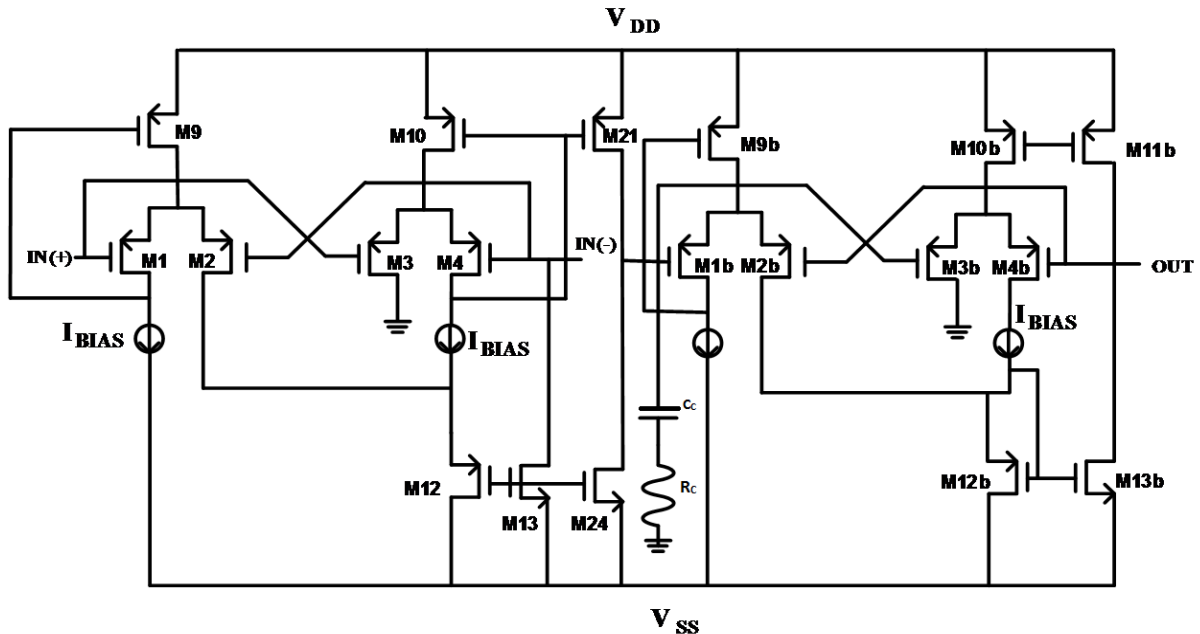


Figure 2. Proposed Architecture.

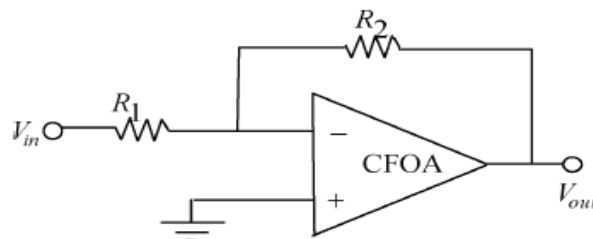


Figure 3. CFOA in inverting configuration.

III. PERFORMANCE COMPARATIVE ANALYSIS OF FIGURES AND TABLES

The proposed architecture shown in figure 2 has number of distinguished features. The number of MOS transistors has been reduced and thus the architecture become much simplified. The aspect ratio of the various transistors used in the proposed architecture has been summarized below in Table I.

TABLE I :TRANSISTOR ASPECT RATIO OF FIGURE 1

TRANSISTOR	W/L
M1-M4, M1b-M4b	180/0.6
M9-M10,M21,M9b-M10b	40/1
M11b	80/1
M12-M13,M24,M12b	130/1
M13b	260/1

III A. SIMULATION

The two proposed solutions have been designed using the 0.35 μ m technology and the results are verified using tanner EDA tool version 14.11. Bandwidth of the modified architecture shown in fig 3. was obtained around 63MHz and 70 MHz for value of the feedback resistor of 3K Ω and 9K Ω respectively. On the other hand, bandwidth in case of base circuit shown in fig 3.2 was coming out to be always more than 2MHz. Thus in our proposed circuit, it can be said that there is a considerable improvement in the bandwidth of the circuit and the bandwidth is always found to be greater than 50MHz. Also, improvement in slew rates and setting time have been reduced. Slew rates was coming out to be 8.1V/ μ sec, which is more than the slew rate obtained for circuit shown in Fig 1. Transistor dimensions of both circuits are summarized in Tables I and II, respectively. The two circuits are here dimensioned for off-chip applications and to account for a larger capacitive load of 20 pF. Also the power supply in both cases are kept equal to 2V. Total harmonic distortion of the modified architecture was found to be almost same as that of the base architecture, but, the number of the MOS used has also been reduced thus the complexity of the circuit had been improved.

TABLE II :COMPARISON OF PERFORMANCE OF THE EXISTING AND PROPOSED CIRCUITS.

PARAMETER	FIG 1.	FIG 3.
Bandwidth	>2MHz	>50MHz
Slew rate	5.2 V/us	8.1 V/us
Offset voltage	4.1 mV	6.7 mV
Settling time	212 ns	134 ns
Technology	350nm	350nm
Supply voltage	2 V	2 V
Load capacitance	20pF	20pF
THD	-76.8 dB	-75.5 dB
Impedence	577 Ω	1.4 K Ω

III B. EXPERIMENTAL RESULTS

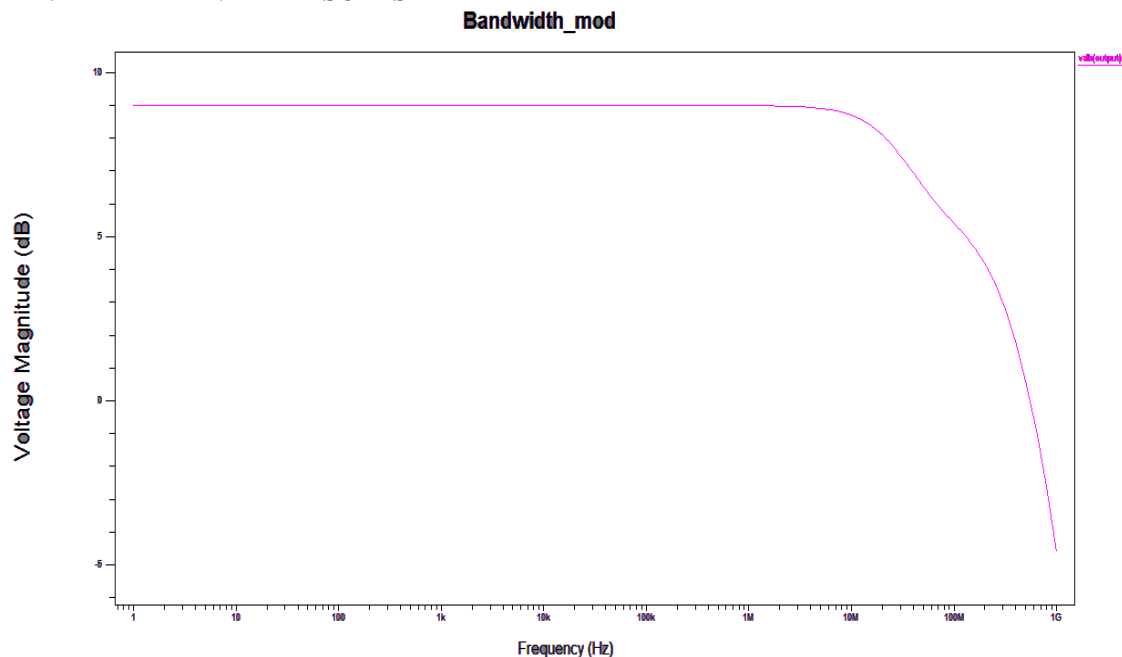


Figure 3. Gain vs Frequency characteristics of proposed circuit.

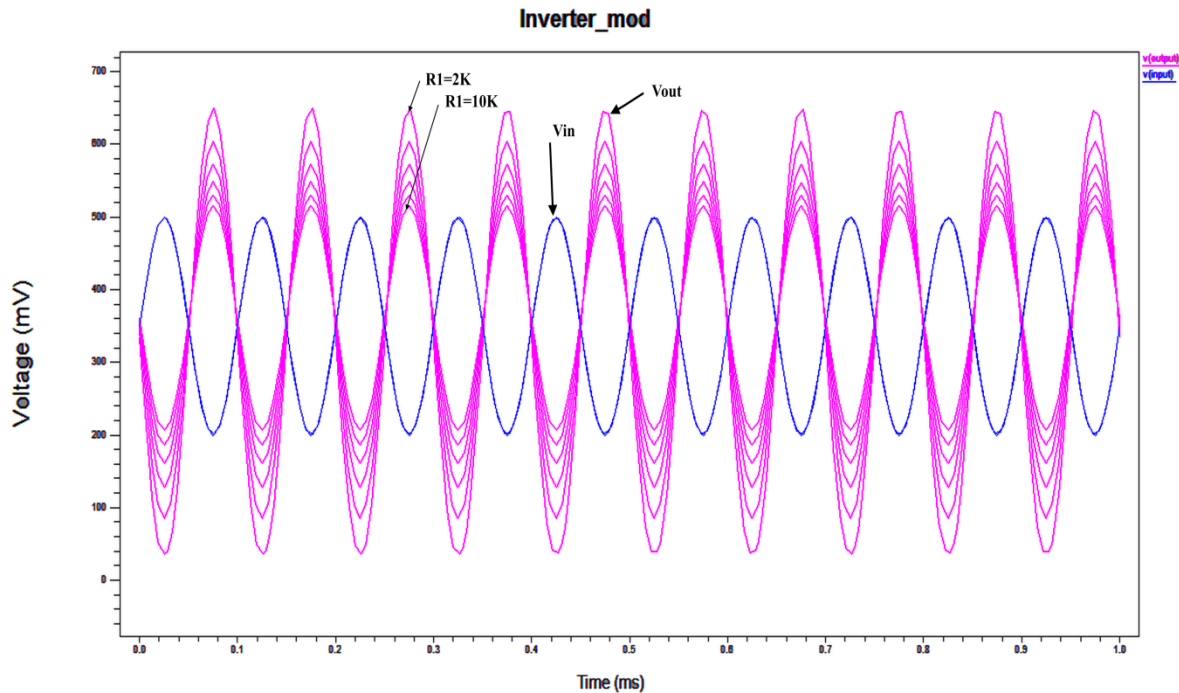


Figure 4. Response of CFOA with improved bandwidth, operating in inverting mode for different value of feedback resistor.

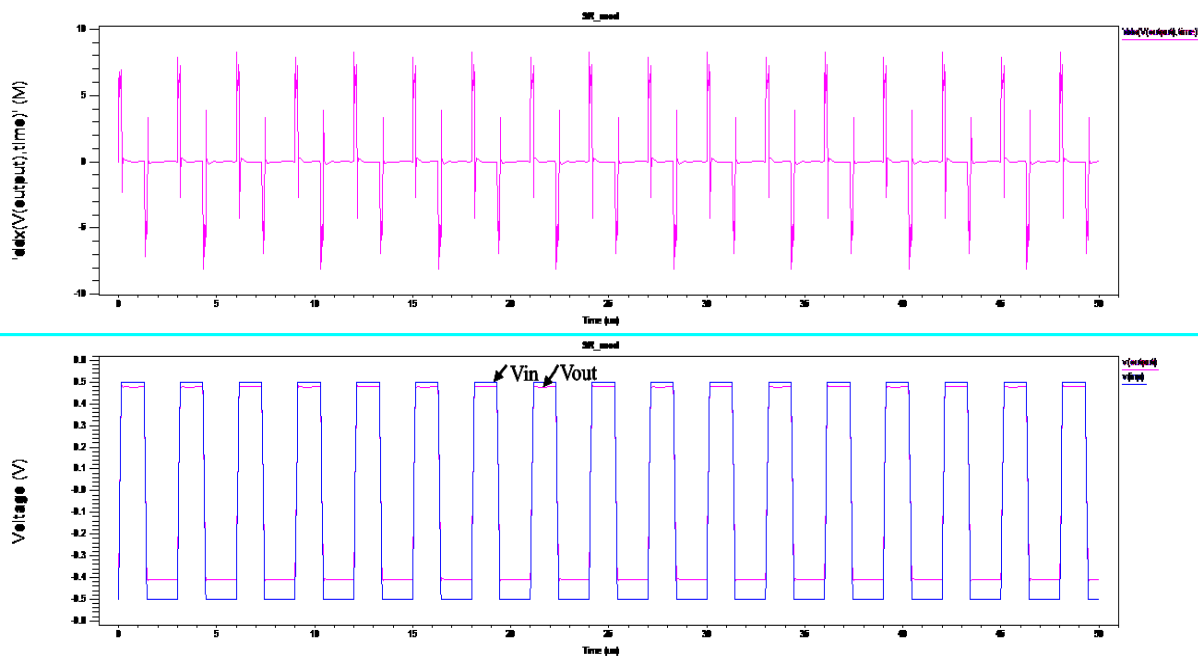


Figure 3. output voltage and slew rate characteristics of proposed circuit.

IV. CONCLUSION

CMOS based current-feedback operational amplifiers with improved bandwidth proposed here. It was obtained from two class AB voltage buffer configurations exploiting local feedback and providing low output resistance and both high current drive and slew-rate capability. Number of improvements in various parameter have been observed and the circuit has also been simplified. Comparison of the proposed circuit with the previous one has been summarized in tabular form. Design examples using a 0.35- μm process were presented and simulations along with experimental results, confirming the effectiveness of the solutions are also provided. The proposed architecture gives high value of offset voltage. Also, circuit is not as stable as its previous counterpart.

REFERENCES

- [1] A. Soliman, "Applications of the current feedback operational amplifiers," *Analog Integrated Circuits Signal Process.*, no. 11, pp. 265–302, 1996.
- [2] S. A. Mahmoud and A. M. Soliman, "New MOS-C biquad filter using the current feedback operational amplifier," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 46, no. 12, pp. 1510–1512, Dec. 1999.
- [3] A. K. Singh and R. Senani, "Active-R design using CFOA-poles: New resonators, filters, and oscillators," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 48, no. 5, pp. 504–511, May 2001.
- [4] J. Bayard and M. Ayachi, "OTA- or CFOA-based LC sinusoidal oscillators-Analysis of the magnitude stabilization phenomenon," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 49, no. 8, pp. 1231–1236, Aug. 2002.
- [5] D. Smith, M. Koen, and A. Witulski, "Evolution of high-speed operational amplifier architectures," *IEEE J. Solid-State Circuits*, vol. 29, pp. 1166–1179, Oct. 1994.
- [6] C. Toumazou and J. Lidge, "Current feedback OpAmps: A blessing in disguise?," *IEEE Circuits Devices Mag.*, pp. 34–37, Jan. 1994.
- [7] Giuseppe Di Cataldo, Alfio Dario Grasso, and Salvatore Pennisi, "two CMOS current feedback operational amplifier"
- [8] S. Pennisi, "High-performance CMOS current-feedback operational amplifier," in *Proc. IEEE ISCAS '05*, Kobe, May 2005, pp. 1573–1576.
- [9] Harvey B., "Current feedback op-amp limitations: a state-of-the-art review" *IEEE International Symposium on Circuits and Systems*, pp. 1062–1069, 1993.
- [10] Smith S.O., "The good, the bad and the ugly: Current feedback technical contributions and limitations" *IEEE International Symposium on Circuits and Systems*, pp. 1058–1061, 1993.
- [11] R. Senani, "Realization of a class of analog signal processing/signal generation circuits: Novel configurations using current feedback op-amps" *Frequenz*, vol. 52, no. 9/10, pp. 196–206, 1998.
- [13] K. Smith, A. Sedra, "The current-conveyor-a new circuit building block," *IEEE Proc.*, vol. 56, pp. 1368–69, 1968.
- [14] A. Sedra, K. Smith, "A second-generation current-conveyor and its applications," *IEEE Trans.*, vol. CT-17, pp. 132–134, 1970.
- [15] R. Senani, D. R. Bhaskar, A. K. Singh, V. K. Singh, "Current Feedback Operational Amplifiers and their Applications" *Springer* New York Heidelberg Dordrecht London, 2013, chapter (3–4).
- [16] Tammam AA, Hayatleh K, Lidgey FJ : "High CMRR current feedback operational amplifier". *Int J Electron* 90:87-97, 2000.
- [17] Tammam AA, Hayatleh K, Han BL, Lidgey FJ: "A Novel current feedback operational amplifier exploiting bootstrapping technique". *Int J Electron* 94: 1157-1170, 2007.
- [18] G. Palumbo, "Bipolar current feedback amplifier: Compensation guidelines," *Analog Integrated Circuits Signal Processing*, vol. 19, no. 2, pp. 107–114, May 1999.
- [19] P. W. Li, M. J. Chin, P. R. Gray, and R. Castello, "A ratio-independent algorithmic analog-to-digital conversion technique," *IEEE J. Solid-State Circuits*, vol. SC-19, pp. 828–836, Dec. 1984.
- [20] B. J. Maundy, A. R. Sarkar, and S. J. Gift, "A new design for low voltage CMOS current feedback amplifiers," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 1, pp. 34–38, Jan. 2006.
- [21] R. Mancini, "Understanding Basic Analog -Active Devices" Application Report SLOA026A - April 2000.

Appendix

The proposed circuit design has been investing the parameters such as bandwidth, slew rate and settling time with the CAD EDA tool. The netlist created and simulate the following extracted parameters such as bandwidth >50MHz, slew rate 8.1V/ μ sec and settling time 134 nsec. The theoretical description of these parameters are described below.

(I) BANDWIDTH

Bandwidth can be defined as a measure of the width of a range of frequencies. It is measured in hertz. It is also defined as the difference between the upper and lower frequencies in a continuous set of frequencies.

If f_H and f_L are the high cutoff and low cutoff frequency respectively, then bandwidth can be given by expression:

$$\text{Bandwidth(B.W)} = f_H - f_L \quad (5)$$

(II) SLEW RATE

Slew rate is defined as the maximum rate of change of output voltage per unit of time and is expressed as volts per second. Limitations in slew rate capability can give rise to non linear effects in electronic amplifiers. Expression for slew rate is given by:

$$SR = \left[\frac{\partial v_o}{\partial t} \right]_{\max} \quad (6)$$

(III) SETTLING TIME

The settling time of an amplifier is defined as the time it takes the output to respond to a step change of input and come into, and remain within a defined error band, as measured relative to the 50% point of the input pulse. Expression for settling time is given by:

$$T_s = 4/\zeta\omega_n \quad (7)$$