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Comparison between the Performance of Basic SEPIC Converter and modified SEPIC Converter with PI Controller

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ABSTRACT: *There are multiple solutions in which line current is sinusoidal. In addition, in the recent years, a great number of circuits have been proposed with non sinusoidal line current. In this paper, a review of the most interesting solutions for single phase and low power applications is carried out. They are classified attending to the line current waveform, energy processing, number of switches, control loops, etc. The major advantages and disadvantages are highlighted and the field of application is found. The paper presents performance analysis of modified SEPIC dc-dc converter with low input voltage and wide output voltage range. The operational analysis and the design is done for the 380W power output of the modified converter. The simulation results of modified SEPIC converter are obtained with PI controller for the output voltage. The results obtained with the modified converter are compared with the basic SEPIC converter topology for the rise time, peak time, settling time and steady state error of the output response for open loop. Voltage tracking curve is also shown for wide output voltage range.*

KEYWORDS: *Dc-dc Power Conversion, SEPIC Converter.*

I. INTRODUCTION

POWER supplies connected to ac mains introduce harmonic currents in the utility. It is very well known that these harmonic currents cause several problems such as voltage distortion, heating, noise and reduce the capability of the line to provide energy. This fact and the need to comply with "standards" or "recommendations" have forced to use power factor correction in power supplies. Unity power factor and tight output voltage regulation are achieved with the very well known two stage approach, shown in Fig. 1. Since the power stage is composed by two converters, size, cost and efficiency are penalized, mainly in low power applications. However, this is probably the best option for ac-dc converters due to the following reasons.

[1] Sinusoidal line current guarantees the compliance of any Regulation.
[2] It gives good performance under universal line voltage.
[3] It offers many possibilities to implement both the isolation between line and load, and the hold-up time.
[4] The penalty on the efficiency due to the double energy processing is partially compensated by the fact that the voltage on the storage capacitor is controlled. The fact of having a constant input voltage allows a good design of the second stage.

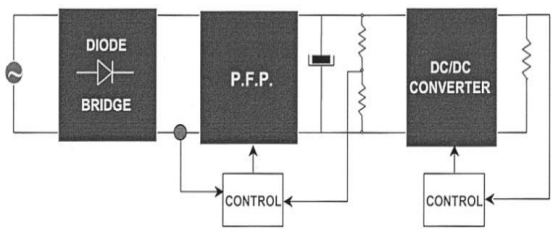


Fig. 1. Two stage ac-dc PFC converter.

Dc-dc converters are widely used in regulated switched mode dc power supplies and in dc motor drive applications. The input to these converters is often an unregulated dc voltage, which is obtained by rectifying the line voltage and it will therefore fluctuate due to variations of the line voltages. Switched mode dc-dc converters are used to convert this unregulated dc input into a controlled dc output at a desired voltage level. The recent growth of battery powered applications and low voltage storage elements are increasing the demand of efficient step-up dc–dc converters. Typical applications are in adjustable speed drives, switch-mode

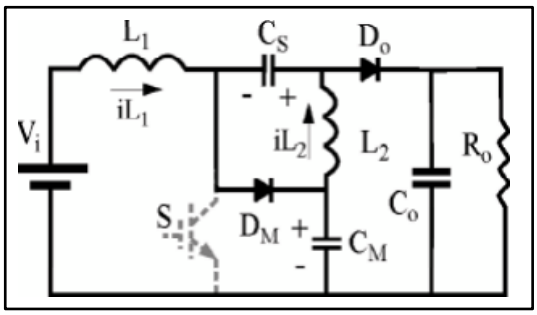


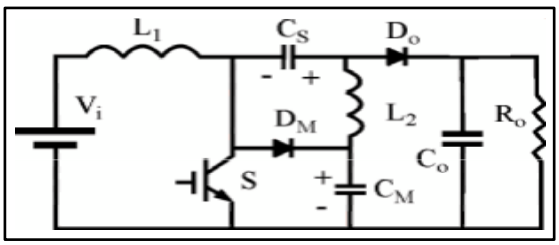
Fig. 2: Circuit of the Modified SEPIC

power supplies, uninterrupted power supplies, and utility interface with nonconventional energy sources, battery energy storage systems, battery charging for electric vehicles, and power supplies for telecommunication systems etc.. These applications demand high step-up static gain, high efficiency and reduced weight, volume and cost. The step-up stage normally is the critical point for the design of high efficiency converters due to the operation with high input current and high output voltage [1]. The boost converter topology is highly effective in these applications but at low line voltage in boost converter, the switching losses are high because the input current has the maximum value and the highest step-up conversion is required. The inductor has to be oversized for the large current at low line input. As a result, a boost converter designed for universal-input applications is heavily oversized compared to a converter designed for a narrow range of input ac line voltage [2]. However, recently new non-isolated dc–dc converter topologies with basic boost are proposed, showing that it is possible to obtain high static gain, low voltage stress and low losses, improving the performance with respect to the classical topologies. Some single stage high power factor rectifiers are presented in [3-6]. A new alternative for the implementation of high step-up structures is proposed in this paper with the use of the voltage multiplier cells integrated with basic non-isolated dc–dc converters. The uses of the voltage multiplier in the basic dc–dc converters add new operation characteristics, becoming the resultant structure well suited to implement high-static gain step-up converters [7]. The use of high static gain and low-switch voltage topologies can improve the efficiency operating with low input voltage, as presented in [8-10].

II. OVERVIEW OF CIRCUIT AND ITS WORKING

The voltage multiplier technique is used to increase the static gain of single-phase boost dc–dc converters. The modified SEPIC converter is accomplished by including of the diode D_M and the capacitor C_M in basic SEPIC converter. An adaptation of the voltage multiplier technique with the SEPIC converter is presented in fig.1. Many operational characteristics of the basic SEPIC converter are changed with the proposed modification. The capacitor C_M is charged with the output voltage of the basic boost converter. Therefore, the voltage applied to the inductor L_2 during the conduction of the power switch S is higher than that in the basic sepic converter, thereby increasing the static gain.

The principle of operation of the modified SEPIC converter presents the following two operation stages. First stage (switch is off) Second stage (switch is on)



The principle of operation of first stage is shown in the fig. 3.

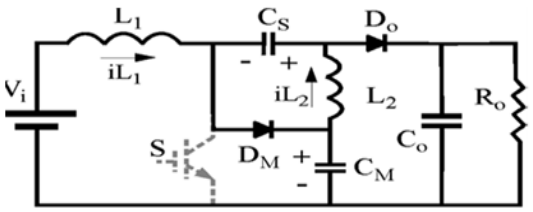


Fig. 3: First Stage (Switch is Off)

The first stage of operation varies from time t_0 to t_1. At the instant t_0, the switch S is turned-off and the energy stored in the input inductor L_1 is transferred to the output through the capacitor C_s and output diode D_o, and also to the capacitor C_M through the diode D_M. Therefore, the switch voltage is equal to the capacitor C_M voltage. The energy stored in the inductor L_2 is transferred to the output through the diode D_o. The principle of operation of second stage is shown in the fig. 4.

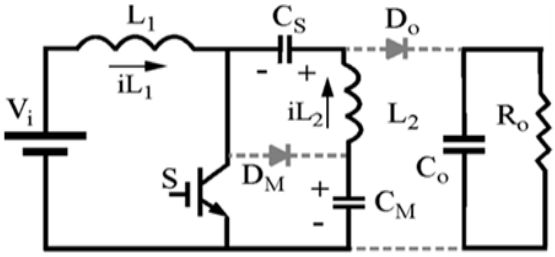


Fig. 4: Second Stage (Switch is ON)

The second stage operation varies from time t_1 to t_2. At the instant t_1, the switch S is turned-on and the diodes D_M and D_o are blocked, and the inductors L_1 and L_2 store energy. The input voltage is applied to the input inductor L_1 and the voltage $V_{CS} - V_{CM}$ is applied to the inductor L_2. The voltage V_{CM} is higher than the voltage V_{CS}.The operating waveforms of modified SEPIC converter are presented in fig. 5. The voltage in all diodes and the power switch is equal to the capacitor C_M voltage. The output voltage is equal to the sum of the voltages across capacitors C_S and C_M respectively. The average L_1 inductor current is equal to the input current and the average L_2 inductor current is equal to the output current [11]. The second stage operation varies from time t_1 to t_2. At the instant t1, the switch S is turned-on and the diodes D_M and D_o are blocked, and the inductors L_1 and L_2 store energy. The input voltage is applied to the input inductor L_1 and the voltage $V_{CS} - V_{CM}$ is applied to the inductor L_2. The voltage VCM is higher than the voltage V_{CS}. The operating waveforms of modified SEPIC converter are presented in fig. 5. The voltage in all diodes and the power switch is equal to the capacitor C_M voltage. The output voltage is equal to the sum of the voltages across capacitors C_S and C_M respectively. The average L_1 inductor current is equal to the input current and the average L_2 inductor current is equal to the output current [11].

III. MODIFIED SEPIC

Static gain is a measure of the ability of a circuit to increase the power from the input to the output. It is usually defined as the ratio of the output to the input of a system. At the steady state for the inductor L_1, the relation presented in (1) occurs:

$$\mathbf{V_i}(\boldsymbol{t_{on}} + \boldsymbol{t_{off}}) = \boldsymbol{V_{CM}}\ \boldsymbol{t_{off}} \text{.....(1)}$$

$$\boldsymbol{V_i D} = (\boldsymbol{V_{CM}} - \boldsymbol{V_i})(\mathbf{1} - \boldsymbol{D}) \text{.....(2)}$$

Therefore, the CM capacitor voltage is defined by (3), which is the same equation of the classical boost static gain given by

$$\frac{\boldsymbol{V_{CM}}}{\boldsymbol{V_i}} = \frac{\mathbf{1}}{\mathbf{1}-\boldsymbol{D}} \text{.....(3)}$$

During the period where the power switch is turned-off (t_{off}), the diodes D_M and D_0 are in conduction state, and the following relation can be defined:

$$\boldsymbol{V_O} = \boldsymbol{V_{CS}} + \boldsymbol{V_{CM}} \text{.....(4)}$$

$$\boldsymbol{V_{CS}} = \boldsymbol{V_O} - \boldsymbol{V_{CM}} \text{.....(5)}$$

The L_2 average voltage is zero at the steady state, and the following relations can be considered
As the basic sepic, boost, and the modified sepic converters present the same input stage, the equation for the determination of the input current ripple is the same for all converters. The input current ripple (Δi_{L1}) during the conduction of the power switch is defined by the following equation.

$$\Delta i_{L1} = \frac{V_i D}{f L_1} \text{.....(6)}$$

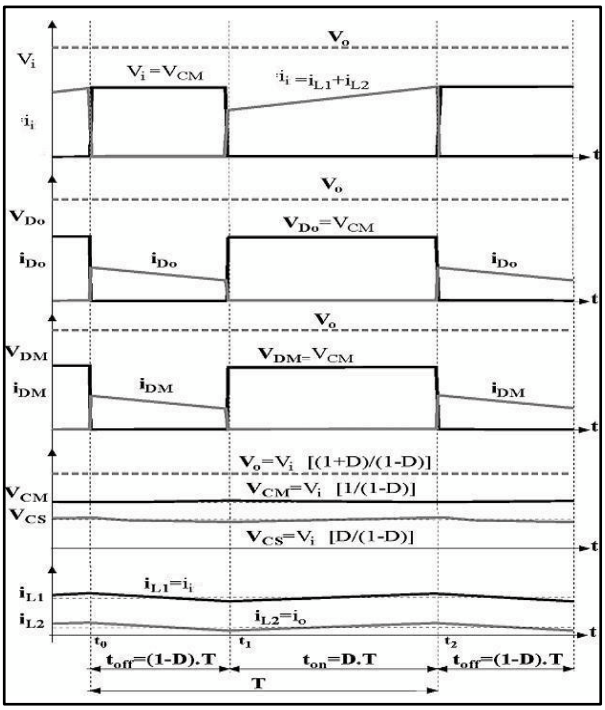


Fig. 5: Steady-State Operation Waveforms

A. Input Current Ripple and L1–L2Inductances

Where, f is the switching frequency.
The input current ripple Δi_{L1} considered is 18% of the peak input current (i_{inpk}). Therefore, the input current ripple is calculated as follows:
$\Delta i_{L1} = i_{inpk} \times 0.18 = 6.5 \times 0.18 = 1.17A$.
The input inductance is calculated for the low input
voltage. The input voltage Vi is 115 V, the converter duty cycle is equal to D = 0.5, with supply frequency 50Hz and switching frequency 48kHz. The input inductance calculated is equal to

$$L_1 = \frac{V_i D}{f \nabla I_{L1}} \text{.....(7)}$$

The input inductance value utilized in the simulation is equal to L_1 = 1mH. As the average input current is higher than the average output current for a step-up converter, the L_2 inductor volume is lower than the L_1 inductor volume. The L_2 inductance utilized in the simulation is half of the L_1 inductance. The L_2 inductance value utilized in the simulation is half of the L_1inductance i.e. L_2= 500µH.

B. Series Capacitor C_s and Multiplier Capacitor C_m

During the power switch turn-on period, the current in the C_S and C_M capacitances is equal to the L_2 inductor current. The capacitor charge variation ΔQ is calculated as

$$\Delta Q = i_{L2} \ DT \text{.....(8)}$$

The high-frequency capacitor voltage ripple ΔV_C can be defined by equation , as a function of the capacitor charge variation. Therefore, the C_S and C_M capacitances can be defined as follows.

$$C = \frac{i_{L2} D}{f \Delta V_C} \text{.....(9)}$$

Where f is the switching frequency and $C=C_S=C_M$

For an input voltage equal to V_i = 115V and a maximum capacitor voltage ripple equal to 7% of the output voltage (ΔV_c = 24.15 V), and the maximum inductor current L_2 is assumed to 1.5A. The capacitors C_S and C_M can be determined from equation

C = 647nF

The capacitors utilized in the analysis of the proposed converter are,

$C = C_S = C_M$ = 660 nF.

C. Output Capacitor C_0

The output filter capacitance is defined by a function of the output power P_o, the supply i.e. grid frequency f_G, and the low frequency output voltage ripple ΔV_o. The output voltage ripple is considered equal to 1% of the output voltage in calculation. The output capacitance is calculated as given below:

$$C_O = \frac{P_O}{2\pi f_G * 2V_O \Delta V_O}$$

The output voltage is calculated from equation. Considering an output voltage ripple equal to 1% of the output voltage for the output power 380W, the output capacitor value is calculated from equation.

Co = 500 µF

IV. RESULT

The designed parameters of the modified SEPIC system is given in Table 1. The closed loop Simulink model for the modified SEPIC converter is shown in fig. 6. The single phase 115V, 50 Hz ac voltage is the input of the SEPIC. The input voltage waveform is shown in fig. 7. The input ac current is in phase with the input voltage waveform having almost unity power factor as shown in fig. 8. The low order harmonics are also absent in the input current, i.e., less current harmonics are injected into the utility. Fig. 9 and fig. 10, are the rectified input voltage and current waveforms respectively. Open loop output voltage waveforms of Basic SEPIC and Modified SEPIC are shown in fig. 11 and fig. 12, respectively. Different open loop parameters of the Basic and Modified SEPIC
are given Table 2. Fig. 13, shows the output voltage stabilization at 345V, 500V and 600V step voltage references at time t=0, t=0.55 and t=0.8s
respectively.

Table 1: Parameters of the Modified SEPIC.

MODEL PARAMETERS	VALUES
INPUT VOLTAGE,Vi	115V
OUTPUT VOLTAGE,Vo	345V
INDUCTOR,L_1	1mH
INDUCTOR,L_2	500µH
SERIES CAPACITOR,C_s	660nF
MULTIPLIER CAPACITOR,C_M	660nF
OUTPUT CAPACITOR,C_o	500µF
SWITCHING FREQUENCY,f_s	48kHz
GRID FREQUENCY,f_G	50Hz

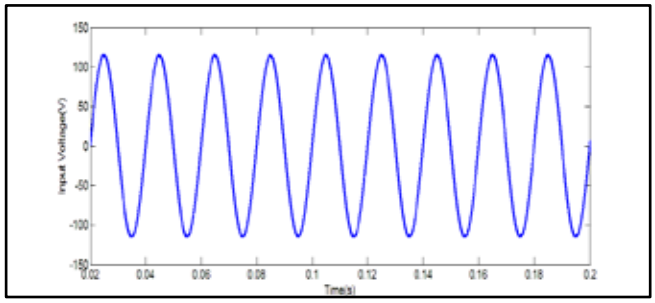


Fig. 6: Input Voltage (115V) Waveform

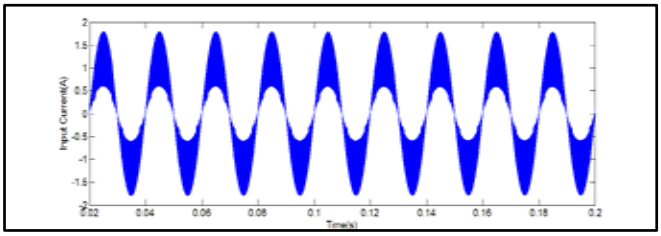


Fig. 7: Input Current Waveform

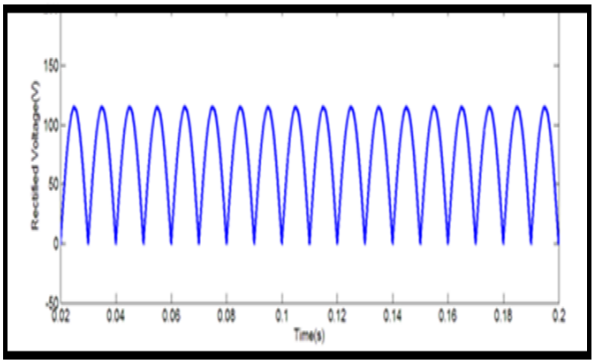


Fig. 8: Rectified Input Voltage Waveform

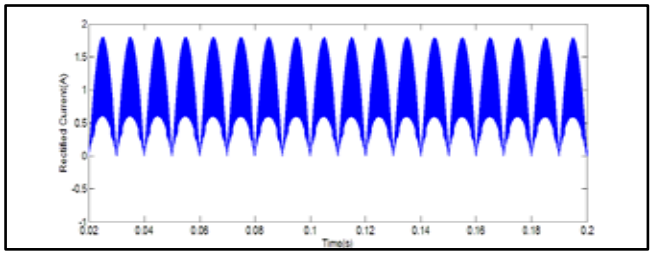


Fig. 9: Rectified Input Current Waveform

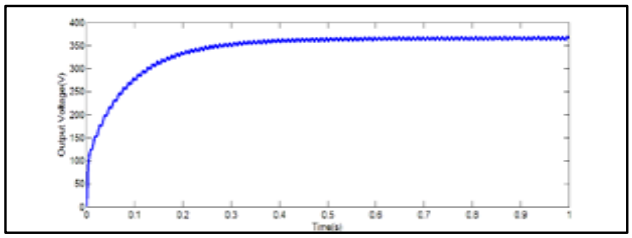


Fig. 10: Output Voltage Waveform of the Basic SEPIC

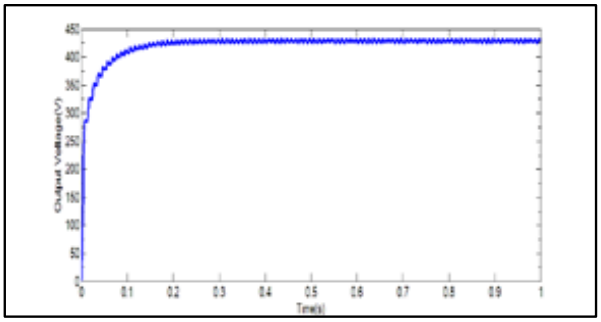


Fig. 11: Output Voltage Waveform of the Modified SEPIC

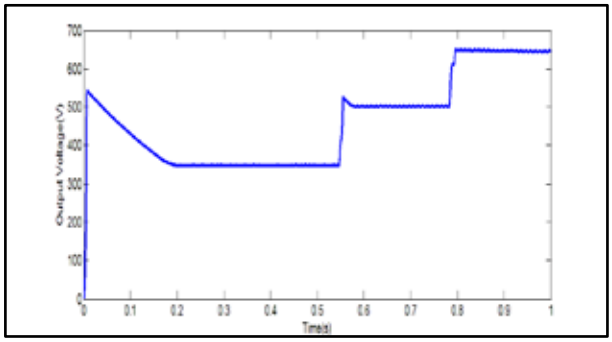


Fig. 12: Output Voltage Variation

V. CONCLUSION

Many proposed solutions for ac-dc power factor correction have been analyzed. They have been classified according to the line current waveform and their performance. If the purpose is to obtain a sinusoidal line current, the classical two-stage approach is the best option, mainly if universal line voltage operation is required. It is desirable to include ZVS if it is feasible to implement it in any or both PFP and dc-dc converter. In general terms, the solutions based on a better energy management (either processing less energy or process it with higher efficiency) do not offer great advantages, unless the efficiency were the unique parameter to consider. Passive solutions are adequate in the low power range for simplicity. A modified SEPIC converter is analyzed and designed. The converter model is simulated on Simulink for open loop as well as closed loop. The PI controller is used to control the output voltage of the modified SEPIC which gives the controlled variation of output voltage from 250V to 650V with input voltage 115V. Although the proposed structure presents a higher circuit complexity than the basic converter but we obtain the higher static gain for the operation with the low input voltage, low switch voltage operation and controlled output voltage variation between 250V and 650V with input voltage 115V with duty ratio 50% with 25kHz switching frequency.

VI. FUTURE SCOPE

The open loop and closed loop models of the modified SEPIC converter may be implemented further for hardware design. There is a classical problem of the reduction of the efficiency due to the additional losses caused by the reverse recovery current of the diodes. This problem is an important source of losses in high power factor rectifiers. This modified SEPIC converter can also be used to reduce the losses associated with the diode reverse recovery current with a regenerative snubbed circuit which can be further implemented.

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