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A Review of Reversible Gates and its Application in Logic Design

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Abstract: - Reversible logic has become one of the most promising research areas in the past few decades and has found its applications in several technologies; such as low power CMOS, nanotechnology and optical computing. The main purposes of designing reversible logic are to decrease quantum cost, depth of the circuits and the number of garbage outputs. The purpose of this paper is to give a frame of reference, understanding and overview of reversible gates **.**In this paper various logic gates and its applicability on logic design have been discussed. Also a brief framework of comparisons between various reversible circuits is presented on the basis of various parameters.

Keywords: - *Reversible logic, Reversible gate, Power dissipation, Garbage, Quantum cost, Reversible Computing.*

I. INTRODUCTION

Energy dissipation is one of the major issues in present day technology. Energy dissipation due to information loss in high technology circuits and systems constructed using irreversible hardware was demonstrated by R. Landauer in the year 1960. According to Landauer's[1] principle, the loss of one bit of information lost, will dissipate kT*ln (2) joules of energy where, k is the Boltzmann's constant, T is the absolute temperature . In 1973, Bennett [2], showed that in order to avoid kTln2 joules of energy dissipation in a circuit it must be built from reversible circuits. According to Moore's law the numbers of transistors will double every 18 months. Thus energy conservative devices are the need of the day. The amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation. Reversible circuits are those circuits that do not lose information. The current irreversible technologies will dissipate a lot of heat and can reduce the life of the circuit. The reversible logic operations do not erase (lose) information and dissipate very less heat. Synthesis of reversible logic circuit differs from the combinational one in many ways.
Firstly, in reversible circuit there should be no fan-out, that is, each output will be used only once.
Secondly for each input pattern there should be unique output pattern. Finally, the resulting circuit must be acyclic. Any reversible circuit design includes only the gates that are the number of gates, quantum cost and the number of garbage outputs.

II. OVERVIEW

Gordon. E. Moore [3] in 1965 predicted that the numbers of components on the chip will double every 18 months. Initially he predicted only for 10 years but due to growth in the integrated-circuit technology his prediction is valid till today. His work is widely recognized as the Moore's law. The effect of Moore's law was studied carefully and researchers have come to the conclusion that as the number of components in the chip increases the power dissipation will also increase tremendously. It is also predicted that the amount of power dissipated will be equal to the heat dissipated by the rocket nozzle. Hence power minimization has become an important factor for today's VLSI engineers.
Landauer [1] stated that the amount of energy dissipated to erase each bit of information is at least kTln2 (where k is the Boltzmann constant and T is the room temperature) during any computation the intermediate bits used to compute the final result are erased. This erasure of bits is one of the main reasons for the power dissipation.

C. H. Bennett [2] in 1973 revealed that the power dissipation in any device can be made zero or negligible if the computation is done using reversible model. He proved his theory with the help of the Turing machine which is a symbolic model for computation introduced by Turing. Bennett also showed that the computations that are performed on irreversible or classical machine can be performed with same efficiency on the reversible machine. The research on the reversibility was started in 1980's based on the above concept.

In the year 1994 Shor [4] did a remarkable research work in creating an algorithm using reversibility for factorizing large number with better efficiency when compared to the classical computing theory. After this the work on reversible computing has been started by more people in different fields such as nanotechnology, quantum computers and CMOS VLSI.

Edward Fredkin and Tommaso Toffoli [5, 6] introduced new reversible gates known as Fredkin and Toffoli reversible gates based on the concept of reversibility . These gates have zero power dissipation and are used as universal gates in the reversible circuits. These gates have three outputs and three inputs, hence they are known as 3*3 reversible gates.

Peres [7] introduced a new gate known as Peres gate. Peres gate is also a 3*3 gate but it is not a universal gate like the Fredkin and Toffoli gate. Even though this gate is not universal gate it is widely used in much application because it has less quantum cost with respect to the universal gate. The quantum cost of the Peres gate is 4.

H Thalpliyal and N Ranganathan [8] invented a reversible gate known as TR gate. The main purpose of introducing this reversible TR gate was to decrease the garbage output in a reversible circuit.

H Thalpliyal and N Ranganathan [9] introduced the reversible logic to sequential circuits. Implementation of the sequential circuit such as D-latch, T latch, JK latch and SR latch using Fredkin and Feynman gate has been done. After this work more research has been done on sequential circuits using reversible gates.

Using the combination of Fredkin and Feynman gate a new gate known as Sayem gate was proposed by Sujata S. Chiwande Prashanth R. Yelekar [10] sayem gate is a 4*4 reversible gate and is used in designing sequential reversible circuits.

M.L. Chuang and C.Y. Wang [11] proposed that the numbers of gates, the number of garbage output were reduced in implementing the Latches and when the results will be compared [9] with 25% improvement was achieved.

Even though some significant works ([12], [13], [14]) have been already done in the field of reversible sequential logic design, research on reversible counters has not been done.

V. Rajmohan and Dr. V. Ranganathan in [15] implemented counters using reversible logic. The synchronous and asynchronous counter designs have the applications in building reversible ALU, reversible processor etc. This work forms an important move in construction of large and complex reversible sequential circuits for quantum computers **.**

III. BASIC DEFINITIONS PERTAINING REVERSIBLE LOGIC

1. The Reversible Logic

The n-input and k-output Boolean function $f(x_1, x_2, x_3 \ldots x_n)$ (referred to as (n, k) function) is called reversible if:

1) The number of outputs is equal to the number of inputs

2) Each input pattern maps to unique output patterns

1.1Reversible Logic Gate

Reversible Gates are circuits in which number of outputs is equal to the number of inputs .And there is a one to one mapping between the vector of inputs and outputs [13][16][17]. It helps to determine the outputs from the inputs as well as helps to uniquely recover the inputs from the outputs.

1.2 Ancilla inputs/Constant inputs

This can be defined as the number of inputs that are to be maintain constant at either 0 or 1 in order to synthesize the given logical function [18]. \

1.3 Garbage Outputs

Additional inputs or outputs can be added so as to make the number of inputs and outputs equal whenever required. This also indicates the number of outputs which are not used in the synthesis of a given function. In certain cases these become mandatory to attain reversibility. Therefore garbage is the number of outputs added to make an n-input k-output function ((n; k) function) reversible.

Constant inputs are used to denote the present value inputs that are added to an (n; k) function to make it reversible. The following simple formula shows the relation between the number of garbage outputs and constant inputs.

Input + constant input = output + garbage. [19]

1.4 Quantum Cost

Quantum cost may be defined as the cost of the circuit in terms of the cost of a primitive gate. It is calculated by the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit. The quantum cost of a

circuit is the minimum number of 2*2 unitary gates to represent the circuit keeping the output unchanged. The quantum cost of a 1*1 gate is 0 and that of any 2*2 gate is the same, which is 1 [20].

2. Reversible Gates

Some of the important reversible logic gates are:

2.1 NOT Gate

The simplest Reversible gate is NOT gate and is a 1*1 gate [21]. The Reversible 1*1 gate is NOT Gate with zero Quantum Cost is as shown in the Figure 1.

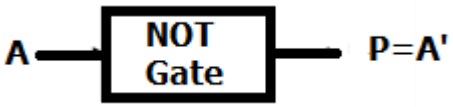

Fig 1: NOT Gate

2.2 CNOT Gate

CNOT gate is also known as controlled-not gate. It is a 2*2 reversible gate. The CNOT gate can be described as: Iv = (A, B) ; Ov = (P= A, Q= A^B) Iv and Ov are input and output vectors respectively. Quantum cost of CNOT gate is 1[22]. Figure 2 shows a 2*2 CNOT gate and its symbol.

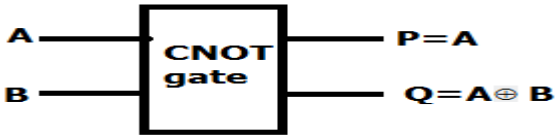

Fig 2: CNOT gate

2.3 Feynman Gate

The Feynman gate which is a 2*2 gate and is also called as Controlled NOT and it is widely used for fan-out purposes. The inputs (A, B) and outputs P=A, Q= A XOR B. It has quantum cost one [23].

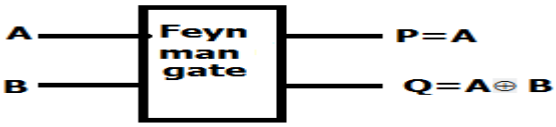

Fig 3: Feynman gate

2.4 Toffoli Gate

Fig 4 shows a 3*3 Toffoli gate. The input vector is I (A, B, C) and the output vector is O(P,Q,R). The outputs are Fig 4 shows a 3*3 Toffoli gate. The input vector is I (A, B, C) and the output vector is O(P,Q,R). The outputs are defined by P=A, Q=B, R=AB ⊕C. Quantum cost of a Toffoli gate is 5[5].

Fig 4: Toffoli gate

2.5 Fredkin Gate

Fig 5 shows a 3*3 Fredkin gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P=A, Q=A′B⊕AC and R=A′C⊕AB. Quantum cost of a Fredkin gate is 5[6].

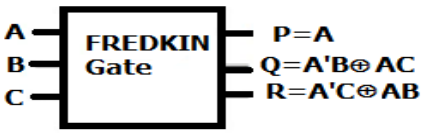

Fig 5: Fredkin Gate

2.6 Peres Gate

Fig 6 shows a 3*3 Peres gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P = A, Q = A⊕B and R=AB⊕C. Quantum cost of a Peres gate is 4[7].

Fig 6: Peres Gate

IV. COMPARATIVE STUDY

To Various reversible gates and different circuits associated with these gates are discussed here. And also comparisons have been made among the existing circuit in terms of various parameters such as quantum cost, garbage output, constant input, gate count and delay. Comparison between existing reversible gates is shown in Table 1.

Table 1. Comparison Between Reversible Logic Gates

Reversible gates	Quantum cost	Types
Feynman gate[23]	1	2*2
Toffoli gate[24]	5	3*3
Fredkin gate[6]	5	3*3
Peres gate[7]	4	3*3
TSG gate[25]	4	4*4
URG gate[26]	unknown	3*3
System gate[27]	unknown	4*4
TR gate[26]	6	3*3
NFT gate[26]	5	3*3
BJN gate[26]	5	3*3
MTSG gate[25]	6	4*4
BME gate[26]	5	4*4
Sayem gate[13]	unknown	4*4
VB-1 gate[28]	unknown	4*4
VB-2 gate[28]	unknown	4*4
MKG gate[29]	unknown	4*4

A comparison has been drawn among the existing reversible full adders shown in Table 2.In the study of [29], a new reversible full adder circuit has been designed that requires only one reversible MKG gate and produces two garbage outputs. In the paper [25], the proposed TSG gate has been used to work singly as a reversible full adder unit producing two outputs. The design in [30] requires five reversible Fredkin gate and produces five garbage outputs. In the paper [31], a reversible full adder circuit have been implemented by two Toffoli and two Feynman gates with 2 garbage outputs. Again, in [32], a new reversible DKG gate has been used to design a reversible full adder. The reversible full adder circuit in [33] requires three reversible gates (two 3*3 new gate and one 2*2 Feynman gate) and produces three garbage outputs. In [34], a single HNG gate has been used to work as a reversible full adder circuit.

Table 2. Comparison between existing Full adders

Name of the circuits	Quantum Cost	Garbage Output	Gate Count	Constant Input
MKG gate based full adder[29]	Not specified	2	1	1
TSG gate based full adder[25]	Not specified	2	1	1
Fredkin gate based full adder[30]	20	3	4	2
Toffoli and Feynman gate based full adder[31]	10	2	4	1
DKG gate based full adder[32]	11	2	Not specified	Not specified
Toffoli, New and Feynman gate based full adder[33]	11	3	3	1
HNG gate based full adder[34]	Not specified	2	1	1

Comparison between existing reversible Full adder/subtractor is shown in Table3.In [32], a new reversible logic gate DKG gate works singly as a reversible full adder circuit with two garbage outputs. In [35], one of the implementations is designed with 3 Feynman gates, 2 Peres gates, 2 TR gates and one Fredkin gate with 7 garbage outputs. Another design is by utilizing 3 TR gates and 6 Feynman gates producing 7 garbage outputs. the third implementation is by using 2 Feynman, 1 Tr and 5 Fredkin gates with 5 garbage outputs. In [37], three designs have been proposed. The first one is by using five Fredkin gate, two Feynman and a TR gate and produces 5 garbage outputs. The second design is by utilizing two Feynman and two TR gates producing 3 garbage outputs. The third is by two FG, two PG gates and produces 3 garbage outputs.

Table3. Comparison between existing Full adder/subtractor

Name of the circuits	Quantum Cost	Garbage Output	Gate Count	Constant Input
DKG gate based full adder/subtractor[32]	Not specified	2	1	1
Fredkin, Feynman, Peres and TR gate based Full adder/subtractor[35]	28	7	8	5
Fredkin and TR gate based full adder/subtractor[35]	24	7	9	5
Feynman, Fredkin and TR gate based full/subtractor[35]	21	5	8	3
Full adder/subtractor circuit 1[36]	Not specified	3	2	2
Full adder/subtractor circuit 2[36]	Not specified	2	1	1
Feynman, Fredkin and TR gate based full adder/subtractor[37]	21	5	8	3
Feynman and TR gate based full adder/subtractor[37]	14	3	4	1
Feynman and Peres gate based full adder/subtractor[37]	11	3	4	1

Comparison between existing reversible BCD adders are made in Table 4.In[38], 8 TSG gates and 3 NG gates are utilized for designing a BCD adder producing 22 garbage outputs. The reversible carry select BCD adder has been designed using 12 TSG, 8 Feynman, 3 NG, 4 Fredkin gates. In the study of[43], a BCD adder has been implemented using 5 HNG gates, 1 Feynman, 1 SCL, and 1 Peres gate.

Table 4. Comparison between existing BCD adders

Name of the circuit	Quantum Cost	Garbage Output	Gate Count	Constant Input	Delay
TSG and NG gate based BCD adder[38]	Not specified	22	11	11	10
BCD adder[22]	70	5	Not specified	1	57
BCD adder[39]	Not specified	22	14	17	13
BCD adder[40]	Not specified	22	23	17	14
BCD adder[41]	55	11	10	7	10
Carry select BCD adder[42]	Not specified	39	27	27	Not specified
BCD adder[43]	Not specified	10	8	6	Not specified
BCD adder[44]	169	8	Not specified	4	Not specified
BCD adder[45]	Not specified	11	9	7	9

Comparison between existing reversible BCD to Excess-3 converters is shown in Table 5.BCD to Excess-3 code converter has been implemented in two different methods in paper [46]. In one method, four HNG gates are used that produces 6 garbage outputs, whereas in the second method, three HNG and one Feynman gates producing 7 garbage outputs. In [47], BCD to Excess-3 code converter has been designed by four TSG gates producing 9 garbage outputs.

Table 5. Comparison between existing BCD to Excess-3 converters

Name of the circuits	Quantum Cost	Garbage Output	Gate Count	Constant Input	Delay
HNG gate based BCD to Excess-3 code converter[46]	24	6	4	6	Not specified
Feynman and HNG gate based BCD to Excess-3 code converter[46]	19	7	4	7	Not specified
TSG gate based BCD to Excess-3 code converter[47]	52	9	4	9	4

Comparison between existing reversible Binary to Gray code converters is shown in Table6.The paper [46] depicts two methods for binary to gray code converter. The first design uses one Feynman and two double Feynman gates producing 3 garbage outputs. The second design utilizes three Feynman gates without any garbage outputs.

Table6. Comparison between existing Binary to Gray code converters

Name of the circuits	Quantum Cost	Garbage Output	Gate Count	Constant Input
Feynman gate based binary to gray code converter[46]	3	0	3	0
Feynman and Double Feynman gate based gray code converter[46]	5	3	3	2

Comparison between existing Comparators by reversible gates is shown in Table 7.

Table 7. Comparison between existing Comparators

Name of the circuits	Quantum Cost	Garbage Output	Gate Count	Constant Input
Feynman, Peres and HNG gate based comparator[46]	42	15	10	11
Comparator[48]	Not specified	23	25	17
Comparator 8 bit[49]	124	36	29	23
Comparator 8 bit[50]	135	42	72	59
Comparator 8 bit[51]	321	64	40	27
Comparator 64 bit[49]	1014	316	253	191
Comparator 64 bit[50]	1143	378	576	Not specified
Comparator 64 bit[51]	2505	512	320	Not specified

Comparison between existing Carry skip adders by reversible gates is shown in Table 8.The Four bit carry skip adder has been implemented using four TSG and four fredkin gates with 12 garbage outputs in the paper [25]. In the study of [52], it is seen that the carry skip adder is designed using two Double Feynman gate, four NFT gate, eight MIG gates producing 19 garbage outputs. In [30], Fredkin gates have been used to produce a carry skip adder with 3 garbage outputs.

Table 8. Comparison between existing Carry skip adders

Name of the circuit	Quantum Cost	Garbage Output	Gate Count	Constant Input
Carry skip adder[52]	Not specified	19	14	15
Carry skip adder[53]	Not specified	22	24	21
Carry skip adder[54]	Not specified	27	22	22
TSG and Fredkin Gate based Carry Skip Adder[25]	Not specified	12	8	7
Fredkin, Peres and MTSG gate based Carry skip adder[55]	Not specified	12	8	7
Fredkin gate based carry skip adder[30]	20	3	4	2

Comparison between existing reversible SR Latches is made in Table 9. In the study of [9], it is seen that the SR latch has been designed by two Peres gates producing two garbage outputs. In the paper [56], SR latch have been designed by using two Fredkin gates producing 2 garbage outputs and also by using two Toffoli gates producing 2 garbage outputs.

Table 9. Comparison between existing SR Latches

Name of the circuits	Quantum Cost	Garbage Output	Gate Count	Constant Input	Delay
Fredkin Gate based SR Latch[56]	10	2	2	Not specified	10
Toffoli Gate based SR Latch[56]	10	2	2	Not specified	10
Peres Gate based SR Latch[9]	8	2	2	2	8

Comparison between existing reversible D Latches is shown in Table 10**.** In the paper [9], the D latch is designed by one Feynman and one Fredkin gate with two garbage outputs. In the paper[28], VB-1 gate works

singly as a D latch. Also, using one VB-1 gate and a Feynman gate, a T Latch have been designed in this paper. In the same paper, JK Latch has been proposed by one VB-1 gate and VB-2 gate producing two garbage outputs. In [57], two Fredkin gates are used to design D Latch.

Table 10: Comparison between existing D Latches

Name of the circuit	Quantum Cost	Garbage Output	Gate Count	Constant Input	Delay
Feynman and Fredkin gate based D latch[9]	7	2	2	1	7
Fredkin gate based D latch[57]	47	6	2	2	25
D latch[58]	10	2	Not specified		10
D latch using VB-1 gate[28]	Not specified	1	1	1	Not specified
T Latch[58]	Not specified	2	2	Not specified	Not specified
T Latch using VB-1 and Feynman gate[28]	Not specified	1	2	1	Not specified
JK Latch[58]	Not specified	3	3	Not specified	Not specified
JK Latch using VB-1 and VB-2 gate[28]	Not specified	2	2	2	Not specified

Comparison between existing reversible Flip Flops is drawn in Table 11.In the paper [28], two VB-1 gates, and a Feynman gate have been used to propose a master slave D Flip-flop. Here, two VB-1 gates and two Feynman gates are utilized to design a master slave T flip-flop, and two VB-1 gates and one VB-2 gate have been used to make a master slave JK flip-flop.

Table 11: Comparison between existing Flip Flops

Name of the circuit	Quantum Cost	Garbage Output	Gate Count	Constant Input	Delay
Master Slave D FF[59]	47	12	Not specified	Not specified	35
Master Slave D FF[60]	13	3	5	2	13
Master Slave D FF[58]	13	4	Not specified	Not specified	13
Master Slave D FF using Fredkin and Feynman gates[18]	12	3	4	2	12
Master Slave D FF using VB-1 and Feynman gate[28]	Not specified	2	3	3	Not specified
Master Slave T FF[60]	83	3			13
Master Slave T FF[58]	17	4			17
Master Slave T FF using Fredkin, Feynman and Peres gate[18]	11	3	4	2	11
Master Slave T FF using VB-1 and Feynman gate[28]	Not specified	2	4	3	Not specified
Master Slave JK FF[60]	39	4			39
Master Slave JK FF[59]	23	5			22
Master Slave JK FF using Fredkin and Feynman gate[18]	18	4	5	2	18
Master Slave JK FF[28]	Not specified	3	3	2	Not specified

Comparison between existing reversible Counters is shown in Table 12. In the study of [61], it is seen that the asynchronous counter had been proposed by using 4 Peres gates and 11 Feynman gates producing 3 garbage outputs. Also, four Peres, six Feynman and two TG have been used to design a synchronous counter have been

Table 12: Comparison between existing Counters

Name of the circuit	Quantum Cost	Garbage Output	Gate Count	Constant Input
Peres and Feynman gate based asynchronous counter[61]	23	4	11	7
Peres, Feynman and Toffoli gate based synchronous counter[61]	32	4	12	7
Asynchronous counter[62]	55	12	8	Not specified
Synchronous counter[63]	35	4	Not specified	Not specified

V. APPLICATIONS OF REVERSIBLE GATES

Reversible computing may have applications in computer security and transaction processing, but the main long-term benefit will be felt very well in those areas which require high energy efficiency, speed and performance .it include the area like

- Low power CMOS.
- Quantum computer.
- Nanotechnology.
- Optical computing.
- DNA computing.
- Computer graphics.
- Communication.
- Design of low power arithmetic and data path for digital signal processing (DSP).
- Field Programmable Gate Arrays (FPGAs) in CMOS technology.

The potential application areas of reversible computing include the following

- Nano computing
- Bio Molecular Computations
- Laptop/Handheld/Wearable Computers
- Spacecraft
- Implanted Medical Devices
- Wallet “smart cards”
- “ Smart tags” on inventory
- Prominent application of reversible logic lies in quantum computers.
- Quantum gates perform an elementary unitary operation on one, two or more two–state quantum systems called qubits.
- Any unitary operation is reversible and hence quantum networks also.
- Quantum networks effecting elementary arithmetic operations cannot be directly deduced from their classical Boolean counterparts (classical logic gates such as AND or OR are clearly irreversible).
- Thus, Quantum computers must be built from reversible logical components.

VI. CONCLUSION

The reversible circuits form the basic building block of quantum computers. This paper presents the primitive reversible gates which are gathered from literature and this paper helps researchers/designers in designing higher complex computing circuits using reversible gates. The paper can further be extended towards the digital design development using reversible logic circuits which are helpful in quantum computing, low power CMOS, nanotechnology, cryptography, optical computing, DNA computing, digital signal processing (DSP), quantum dot cellular automata, communication, computer graphics.

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REFERENCES

[1] R. Landauer, - Irreversibilty and Heat Generation in the Computational Process, *IBM Journal of Research and Development, 5*, pp. 183-191, 1961

[2] Bennett C.H., “Logical reversibility of Computation”, IBM J.Research and Development, pp. 525-532, 1973.

[3] Gordon. E. Moore, *Cramming more components onto integrated circuits Electronics, Volume 38, Number 8*, April 19, 1965.

[4] P. Shor, Algorithms for quantum computation: discrete log and factoring, Proc. 35th Annual Symp. On Found. Of Computer Science (1994), IEEE Computer Society, Los Alamitos, 124-34.

[5] E. Fredkin, T Toffoli, "Conservative Logic", International Journal of Theor. Physics, 21(1982), pp. 219-253

[6] T. Toffoli., Reversible Computing, Tech memo MIT/LCS/TM-151, MIT Lab for Computer Science (1980).

[7] A. Peres, Reversible Logic and Quantum Computers, Physical Review A, vol. 32, pp. 3266-3276, 1985.

[8] H Thapliyal and N Ranganathan, "Design of Efficient Reversible Binary Subtractors Based on a New Reversible Gate", IEEE Proceedings of the Computer Society Annual Symposium on VLSI, pp. 229-234 (2009).

[9] H Thapliyal and N Ranganathan, "Design of Reversible Latches Optimized for Quantum Cost, Delay and Garbage Outputs", Proceedings of Twenty Third International Conferences on VLSI Design, pp. 235-240(2010)

[10] Sujata S. Chiwande and Prashanth R. Yelekar, Design of sequential circuit using reversible logic, IEEE-International Conference Advances in Engineering, Science and Management (ICAESM -2012) March30, 31, 2012.

[11] M. L. Chuang and C.Y. Wang, Synthesis of reversible sequential elements, ACM journal of Engineering Technologies in Computing Systems (JETC), vol. 3, no. 4, 2008.

[12] P. Picton, "Multi-valued sequential logic design using Fredkin gates," Multiple-Valued Logic Journal, Vol. 1, pp. 241-251, 1996.

[13] Abu Sadat Md. Sayem and Masashi Ueda, "Optimization of Reversible Sequential Circuits," Journal of Computing, vol.2, issue 6, pp. 208-214, 2010.

[14] SKS Hari, S Shroff, Sk Noor Mahammad and V. Kamakoti, "Efficient Building Blocks for Reversible Sequential Circuit design," Proceedings of the International Midwest Symposium on Circuits and Systems, 2006.

[15] V.Rajmohan, V.Ranganathan, "Design of counter using reversible logic" 978-1-4244-8679-3/11/$26.00 ©2011 IEEE.

[16] Babu HMH, Islam MR, Chowdhury AR, Chowdhury SMA. — Synthesis of full-adder circuit using reversible logic, 17th International Conference on VLSI Design 2004, 757-60.

[17] Ashis Kumer Biswas, Md. Mahmudul Hasan, Moshaddek Hasan, Ahsan Raja Chowdhury and Hafiz Md. Hasan Babu. "A Novel Approach to Design BCD Adder and Carry Skip BCD Adder", 21st International Conference on VLSI Design, 1063-9667/08 © 2008 IEEE DOI 10.1109/VLSI.2008.37.

[18] H.Thapliyal and N. Ranganathan, — Design of reversible sequential circuits optimizing quantum cost, delay and garbage outputs, ACM Journal of Emerging Technologies in Computing Systems, vol. 6, no.4, Article 14, pp. 14:1–14:35, Dec. 2010.

[19] B.Raghu kanth, B.Murali Krishna, M. Sridhar, V.G. Santhi Swaroop "A Distinguish Between Reversible And Conventional Logic GATES" , *International Journalof Engineering Research and Applications (IJERA) Vol. 2, Issue 2*,Mar-Apr 2012, pp.148-151

[20] J. Smoline and David P. DiVincenzo, "Five Two-Qubit Gates Are Sufficient To Implement The Quantum Fredkin Gate", *Physics Review A, vol. 53, no.4*, pp. 2855-2856,1996.

[21] B.Raghu kanth, B.Murali Krishna, M. Sridhar, V.G. Santhi Swaroop "A Distinguish Between Reversible And Conventional Logic Gates", *International Journal of Engineering Research and Applications (IJERA) , Vol. 2, Issue 2*,Mar-Apr 2012, pp.148-151

[22] Himanshu Thapliyal, Nagarajan Ranganathan, "A new Reversible Design of BCD Adder" ‖9783981080179/DATE11/@2011 *EDAA*

[23] R. Feynman, "Quantum Mechanical Computers", *Optical News. 1985*, pp. 11-20

[24] Prashant. R.Yelekar; Prof. Sujata S. Chiwande "Introduction to Reversible Logic Gates & its Application" 2nd National Conference on Information and Communication Technology (NCICT) 2011 *Proceedings published in International Journal of Computer Applications® (IJCA)*
Thapliyal H, M. B.S. Shrinivas." A New Reversible TSG Gate and Its Application for Designing Efficient Adder Circuits". *Centre for VLSI and Embedded System Technologies International Institute of Information Technology, Hyderabad*, 500019, India

[25] Raghava Garipelly, P. Madhu Kiran, A. Santosh Kumar, "A review on reversible logic gates and their implementation*", IJETAE ISSN 2250-2459, Vol. 3* pp. 417-423

[26] Pradeep singla and Naveen kr. Malik, "A Cost - Effective Design of Reversible programmable logic array" *International Journal of Computer Application, volume 41 – no. 15*, march- 2012.

[27] Bhagyalakshmi H R, Venkatesha M K "Design of Sequential Circuit Elements Using Reversible Logic Gates" *World Applied Programming, Vol (2), Issue (5), May 2012. 263-271*

[28] Majid Haghparast and Keivan Navi "A Novel Reversible Full Adder Circuit for Nanotechnology Based Systems" *Journal of Applied Sciences Vol. 2(24),* pp.3995-4000, 2007

[29] J .W. Bruce, M.A. Thornton, L. Shivakumaraiah, P.S. Kokate, andX. Li, "Efficient Adder Circuits Based on a Conservative Reversible Logic Gate", *IEEE Computer Society Annual Symposium on VLSI, April 25-26,* 2000, Pittsburgh, Pennsylvania.

[30] M. Perkowski, Lech Jozwiak, Pawel Kerntopf, Alan Mishchenko,Anas Al-Rabadi, "A General Decomposition for Reversible Logic", *In 5th International Red-Muller Workshop, pages* 119-138,2001

[31] Krishnaveni D. D. and N. Geetha Priya, "Novel design of reversible serial and parallel adder/subtractor*" International Journal of Engineering Science and technology*, 2011

[32] Md. M. H Azad Khan, "Design of Full-adder With Reversible Gates", *International Conference on Computer and Information Technology, Dhaka, Bangladesh,* 2002, pp. 515-519

[33] M. Haghparast, S. J. Jassbi, K. Navi and O. Hashemipour, "Design of a Novel reversible Multiplier Circuit using HNG Gate in Nanotechnology ", World Applied Sci. J., Vol. 3, pp. 974-978, 2008

[34] V.Kamalakannan1, Shilpakala.V2, Ravi. H.N "Design of adder / subtractor circuits based on reversible gates" *An ISO 3297: 2007 Certified Organization) Vol. 2, Issue 8,* August 2013

[35] Islam, M.S. et a!., "Low cost quantum realization of reversible multiplier circuit", *Information technology journal,8(2009)*208

[36] Rangaraju H G, Venugopal U, Muralidhara K N, Raja K B, "Low Power Reversible Parallel Binary Adder/Subtractor"

[37] H.Thapiyal, S.Kotiyal, M.B.Srinivas, "Novel BCD adders and their reversibe logic implementation for IEEE 754r format" *Proceedings of the 19th International Conference on VLSI design,* 3-7 January, 2006.

[38] Haghparast M. and K. Navi, 2008. A Novel reversible BCD adder for nanotechnology based systems. *Am. J. Applied Sci., 5 (3):* 282-288

[39] Hafiz Md. Hasan Babu and A. R. Chowdhury, "Design of a Reversible Binary Coded Decimal Adder by Using Reversible 4-bit Parallel adder", *VLSI Design 2005,* pp-255-260, Kolkata, India, Jan 2005.

[40] K.Biswas,et.al., "Efficient approaches for designing reversible Binary Coded Decimal adders'' *Microelectron,J(2008)* doi:10.10.16/j.mejo.2008.04.003

[41] K.Susan Christina "Realization of BCD adder using Reversible Logic." *International Journal of Computer Theory and Engineering, Vol. 2, No. 3,* June, 2010 1793-8201

[42] H.R.Bhagyalaxmi, M.K. Venkatesha, "Optimized Reversible BCD adder using New Reversible Logic gates", Journal *of Computing, Vol. 2,* pp.28-32, 2010

[43] M. Thomsen and R.Gluck, "Optimized reversible binary-coded decimal adders," *J. Syst. Archit., vol. 54, no. 7,* pp. 697–706, 2008.

[44] James.R.K; Shahana, T.K.; Jacob, K.P.; Sasi, S. "A New Look at Reversible Logic Implementation of Decimal Adder", *System on-Chip, The International Symposium on System-on-Chip Tampere, Finland Nov 20-22,* 2007 Year 2007.

[45] Majid Haghparast, Maryam Hajizadeh, Rogayye Hajizadeh and 2Rozhin Bashiri "On the Synthesis of Different Nanometric Reversible Converters", *Middle-East Journal of Scientific Research 7 (5):* 715-720, 2011 ISSN 1990-9233 © IDOSI Publications, 2011

[46] Himanshu Thapiyal, and Hamid R. Arbania, R. Bajpayi and kamal K. Sharma, "Partial Reversible gates (PRG) for reversible BCD Arithmetic".

[47] Lihui Ni, Xiaoyu Dai, Zhijin Guan and Wenjuan Li, "Using new designed NLG gate for the realization of four-bit reversible numerical comparator" *International Conference on Educational and Network Technol., (ICENT 2010)* pp: 254 - 258.

[48] Morrision, Mathew Lewandowsky, and Nagarajan Ranganasthan, "Design of a Tree Based Comparator and Memory Unit Based on a Novel Reversible Logic Structure",*VLSI(ISVLSI),2012 IEEE Computer Society Annual Symposium on.IEEE,*2012.

[49] H Thapliyal, N Ranganathan and Ryan Ferreira, "Design of a Comparator Tree based on Reversible logic*," Proceedings of Tenth IEEE International Conference on Nanotechnology Joint Symposium with Nano,* August 2010, pp. 1113 – 1116.

[50] A.N. Al-Rabadi "Closed System Quantum logic network implementation of the Viterbi algorithm", *Facta Universitatis-Ser: Elec. Energy, Vol 22, No. 1,* pp.1-33, April, 2009

[51] Islam, M.S., M.M. Rahman, Z. Begum and M.Z. Hafiz, 2009. Fault tolerant reversible logic synthesis: Carry look-ahead and carry-skip adders. *Proceedings of the International Conference on Advances Computational Tools for Engineering Applications,* Jul. 15-17, IEEE Xplore Press, Zouk Mosbeh, pp: 396-401. DOI: 10.1109/ACTEA.2009.5227871(Bruce et al., 2002)

[52] Lala, P.K., J.P. Parkerson and P. Chakraborty, 2010. Adder designs using reversible logic gates. *WSEAS Trans. Circ. Syst.*, 9: 369-378.
[53] Hafiz Hasan Babu, Rafiqul Islam, Ahsan Raza Chowdhury, Syed Mostahed Ali Chowdhury. "Reversible Logic Synthesis for Minimization of Full-Adder Circuit." *Euromicro Symposium on Digital Systems Design (DSD'03),* September 01-06, 2003, Belek-Antalya, Turkey.
[54] J. E. Rice. An introduction to reversible latches. *Comput. J.*, 51(6):700–709, 2008
[55] Himanshu Thapliyal and M. B. Srinivas. An extension to DNA based fredkin gate circuits: "design of reversible sequential circuits using fredkin gates". *In Proc. SPIE 6050, 60500O*, 2005
[56] Thapliyal, H. And Vinod, A. P. 2007. Design of reversible sequential elements with feasibility of transistor implementation. In *Proceedings of the IEEE International Symposium on Circuits and Systems.* 625–628
[57] J. Rice. A new look at reversible memory elements. *In Proc. Intl. Symp. on Circ. and Sys. (ISCAS)* 2006, pages 243–246, Kos, Greece, May 2006**.**
[58] M. Choung and C. Wang, *ACM Journal on emerging technologies in computing systems*, 3(2008) 19.1.
[59] Md. Selim Al. Mamun, B.K. Karmakar, "*Design of reversible counter" International journal of advanced computer science and applications, Vol. 5, No. 1*, 2014-04-03
[60] V. RajMohan, V. Ranganathan, "*Design of counter using reversible logic*" 978-1-4244-8679-3/11/$26.00 ©2011 IEEE
[63] Mozannel, H. A. Khan and Marek Perkowski, "Synthesis of reversible synchronous counters", 2011 41st *IEEE International Symposium on Multiple-Valued Logic*, 0195-623.