

Comparative Analysis of Total Harmonic Distortion (THD) of Sinusoidal Pulse-width Modulation Technique using Single-phase Seven-level Diode-Clamped Multi-level Inverter

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ABSTRACT: In this paper a comparative analysis of various Sinusoidal Pulse-width Modulation Techniques determine THD using Single-phase Seven-level Diode-clamped Multi-level Inverter was carried out. The analysis of THD of the multi-level inverter is performed using the phase opposition disposition (POD), and phase disposition (PD), SPWM switching control techniques at varying modulation index (m_i) of 0.6 to 1.0. The result obtained from MATLAB/SIMULINK simulation for THD of the DCMLI using PD SPWM for modulation index of 0.6 to 1.0 shows that the POD SPWM has the lowest THD of 17.92 % at a modulation index of 1.0.

Keywords: Phase Disposition (PD), Phase Opposition Disposition (POD), Pulse Width Modulation (PWM), Total Harmonic Distortion (THD) Sinusoidal Pulse Width Modulation Technique (SPWM).

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I. INTRODUCTION

The use of multilevel inverter has grown significantly in many industrial power applications[9]. Multilevel inverters have very attractive attributes as they generate low harmonic component at low switching frequency. They also operate at lower losses and low Electro-Magnetic Interface (EMI). Inverter as a device converts the DC supply of the battery into AC power supply required by most of the electrical/electronic equipments [8]. The process through which the Inverter converts DC power supply to AC power supply is called *inversion*. This inversion process is the reverse of the rectifier process, where the AC supply is converted into DC power supply.

The design of inverting circuit depends on the input voltage, output voltage and frequency of an inverter. A power inverter can be entirely electronic or may be a combination of mechanical effects and electronic circuits [1]

Multi-level converters (MLCs) offer several advantages in terms of high power capability, transformer less operation, short-circuit protection, and excellent quality of output current waveform [2]

There are different types of power converters which include: DC-DC converters (chopper), DC-AC converters (inverters), AC-DC converters (rectifiers) and AC-AC converters (converter) [3]. Converters can come in many different varieties, differing in price, power, efficiency and purpose. Recently, converters have become more and more common over the past several years as support for self-sufficient power has increased [4].

Multilevel power conversion is used to provide more than two voltage level to achieve smoother and less distorted DC to AC power conversion and it can generate multiple steps voltage waveform with less distortion, less switching frequency and higher efficiency.

Multi-Level Inverter (MLI) topologies have been widely used in the motor drive industry to run induction machines for high power and high voltage configurations [5].

MLI's divide the main dc supply voltage into several dc sources which are used to synthesize an AC voltage into a stepped approximation of the desired sinusoidal waveform. The number of stages (cells or capacitors depending on the respective topology) help decide the power capacity of the inverter as a whole. Suitable connections either in series or shunt mode or both are done to achieve higher voltage and/or current ratings. Multi-level converters (MLCs) offer several advantages in terms of high power capability, transformer-

less operation, short-circuit protection, and excellent quality of output current waveform [2]. There are basically three main commercial topologies of multilevel voltage source inverters which include: Diode-clamped (Neutral Point Capacitor MLI), Flying Capacitor (FC-MLI) and Cascaded H-Bridge (CHB-MLI)[9]

The diode-clamped MLI is used due to its high power applications and the diode-clamped inverter has a relatively simple control and implementation methods. The main advantages of this configuration are better efficiency, less harmonic distortion due to more voltage levels and half of voltage rating of switching devices [10].

1.1 Multi-Level Inverters

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II. DESIGN AND ANALYSIS

2.1 System Block Diagram

Fig. 1 shows the block diagram of a single phase seven level Diode Clamp multi-level inverter. The battery bank array generates the required DC voltage of $220V_{dc}$ that the boost converter steps up to $630V_{dc}$ which is controlled by PI controller for error handling. The step up voltage is fed into a single phase seven level Diode Clamp MLI using optimized SPWM to generate switching pulses for the inverter switches which produce a seven level output voltage of $220V_{ac}$ for household load consumption.

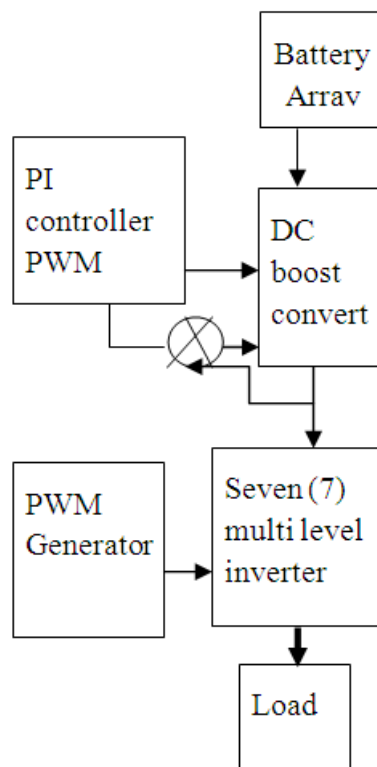


Figure 1: The block diagram of the single phase seven level Diode Clamp inverter.

2.2 Circuit Configuration and Operational Principle

The circuit in Fig. 2 shows a single phase five level DCMLI which uses twelve (12) power semiconductor switches, six (6) (n-1) where n=7, DC link capacitors and ten (10) clamping diodes. This DCMLI consists of six switching pairs (S_1, S_7), (S_2, S_8), (S_3, S_9), (S_4, S_{10}), (S_5, S_{11}) and (S_6, S_{12}). If one switch of the pair

is switched on, the other complementary switch of same pair must be off. The DC-link capacitors together with the diodes clamp the switching voltage to half level of the DC bus voltage while the neutral (N) is the reference point of the circuit. Typical switch combinations to obtain the required output voltage levels for seven-level DCMLI are as shown in Table 1.

In the circuit configuration of the single phase seven level DCMLI, each inverter phase is powered by a single DC source. With the appropriate switching of the semi-conductor switches in the modules, each of the phases produces seven output voltage levels. The switching patterns for the different voltage levels are as presented in Table 1.

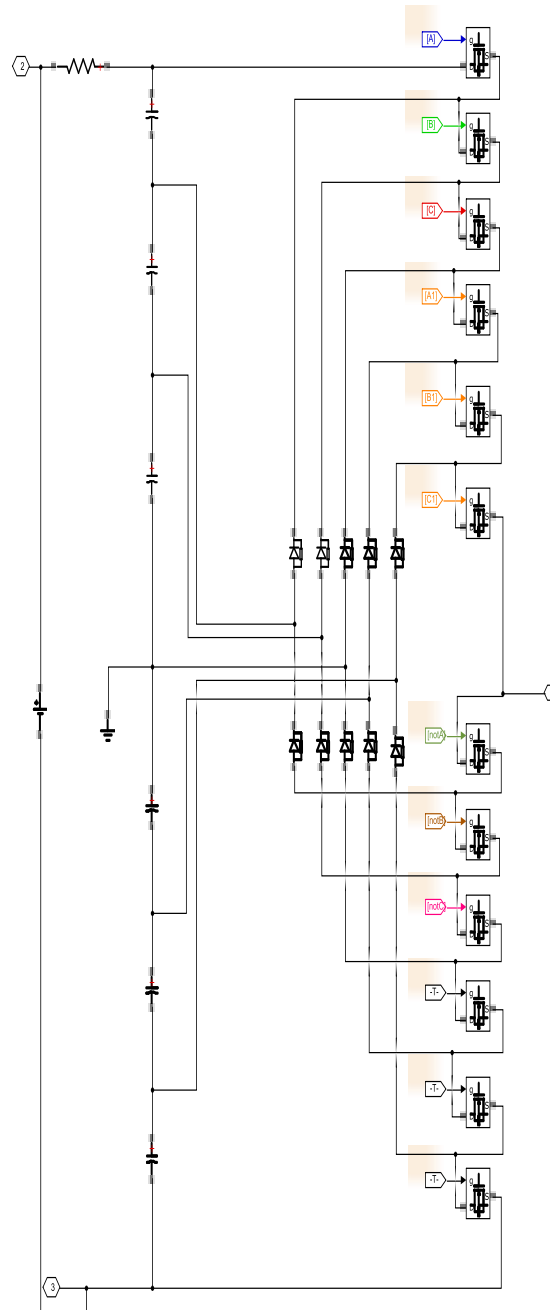


Figure 2: Single-phase Seven-Level Diode Clamped MLI

Table 1: Switching states of a Seven-level DC MLI

Output Voltage Level	Switching States											
	S ₁	S ₂	S ₃	S ₄	S ₅	S ₆	S ₇	S ₈	S ₉	S ₁₀	S ₁₁	S ₁₂
Vdc/2	1	1	1	1	1	1	0	0	0	0	0	0
Vdc/3	0	1	1	1	1	1	1	0	0	0	0	0
Vdc/6	0	0	1	1	1	1	1	1	0	0	0	0
0	0	0	0	1	1	1	1	1	1	0	0	0
-Vdc/6	0	0	0	0	1	1	1	1	1	1	0	0
-Vdc/3	0	0	0	0	0	1	1	1	1	1	1	0
-Vdc/2	0	0	0	0	0	0	1	1	1	1	1	1

III. DESIGN OF INVERTER CONTROL CIRCUIT

The Modeling of Switching Logic Equations

The operation of a traditional single-phase seven level diode clamped inverter requires six carrier ($n - 1 = 7 - 1 = 6$) signals and a single modulating waveform. These signals combine to produce pulses for the switching of the twelve inverter switches. The analysis of the combination of the signals is as follows [7].

In equation 25 to 48 that follows, G is the modulating signal $m(t)$, A is the pulse obtained when the modulating signal $m(t)$ and the carrier signal $r_1(t)$ with [10 12] output values are compared, A_1 is the pulse produced when $m(t)$ and $r_2(t)$ with [8 10] output values are compared, A_2 is the resulting pulse when $m(t)$ and $r_3(t)$ with output values [6 8] are compared, B pulse results when $m(t)$ and $r_4(t)$ with [4 6] output values are compared, when $m(t)$ and $r_5(t)$ [2 4] are compared B_1 pulse is produced, B_2 is the pulse obtained by comparing $m(t)$ and $r_6(t)$ with [0 2] values. The combination of these pulses trigger the switches numbered from S_1 to S_{12} .

The equations developed from the analysis of the signals are given by equations (1) to (12). [7]

$$S_1 = A \cdot \bar{G} + \bar{A} \cdot G \tag{1}$$

$$S_4 = A \cdot G + \bar{A} \cdot \bar{G} \tag{2}$$

$$S_5 = A_1 \cdot \bar{G} + \bar{A}_1 \cdot G \tag{3}$$

$$S_8 = A_1 \cdot G + \bar{A}_1 \cdot \bar{G} \tag{4}$$

$$S_9 = A_2 \cdot \bar{G} + \bar{A}_2 \cdot G \tag{5}$$

$$S_{12} = A_2 \cdot G + \bar{A}_2 \cdot \bar{G} \tag{6}$$

$$S_3 = B \cdot \bar{G} + \bar{B} \cdot G \tag{7}$$

$$S_2 = B \cdot G + \bar{B} \cdot \bar{G} \tag{8}$$

$$S_7 = B_1 \cdot \bar{G} + \bar{B}_1 \cdot G \tag{9}$$

$$S_6 = B_1 \cdot G + \bar{B}_1 \cdot \bar{G} \tag{10}$$

$$S_{11} = B_2 \cdot \bar{G} + \bar{B}_2 \cdot G \tag{11}$$

$$S_{10} = B_2 \cdot G + \bar{B}_2 \cdot \bar{G} \tag{12}$$

The modulation circuit for the single-phase of the inverter is designed using De Morgan's laws as shown in equations (13) to (24).

$$S_1 = A \oplus \bar{G} \tag{13}$$

$$S_4 = \bar{A} \oplus G \tag{14}$$

$$S_5 = A_1 \oplus \bar{G} \tag{15}$$

$$S_8 = \bar{A}_1 \oplus G \tag{16}$$

$$S_9 = A_2 \oplus \bar{G} \tag{17}$$

$$S_{12} = \bar{A}_2 \oplus G \tag{18}$$

$$S_3 = B \oplus \bar{G} \tag{19}$$

$$S_2 = \bar{B} \oplus G \tag{20}$$

$$S_7 = B_1 \oplus \bar{G} \tag{21}$$

$$S_6 = \bar{B}_1 \oplus G \tag{22}$$

$$S_{11} = B_2 \oplus \bar{G} \tag{23}$$

$$S_{10} = \bar{B}_2 \oplus G \tag{24}$$

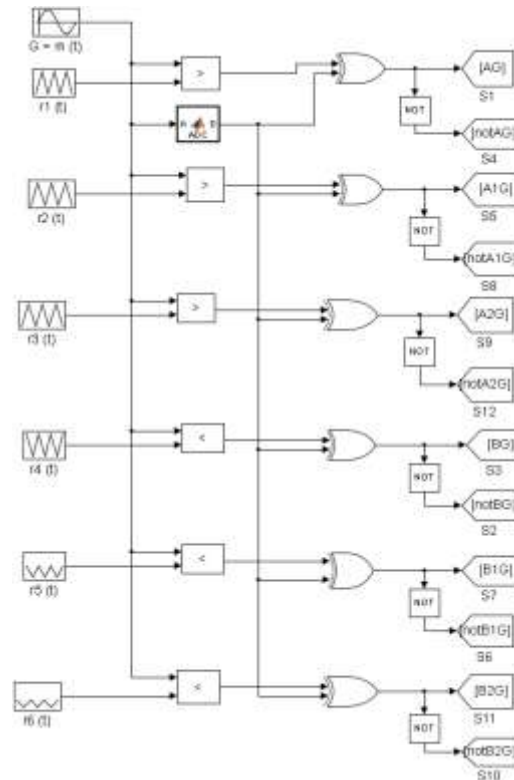


Figure 3: Sinusoidal reference and triangular carrier waves of APOD SPWM for gating pulses

IV. THD SIMULATION OF THE SINGLE-PHASE SEVEN LEVEL DCMLI FOR PD AND POD AT M.I = 0.6 TO 1.0 USING MATLAB/SIMULINK

The THD for the DCMLI was simulated for PD and POD SPWM techniques at varying modulation index of 0.6 to 1.0. The waveforms are as presented in Fig. 4 to Fig. 7.

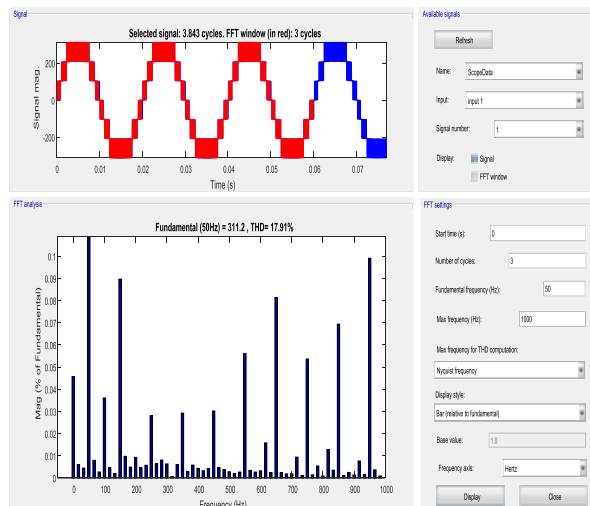


Figure 4: Voltage Output of a Single-Phase Seven-Level DCMLI on no load at m=0.1 to 0.6 for PD PWM

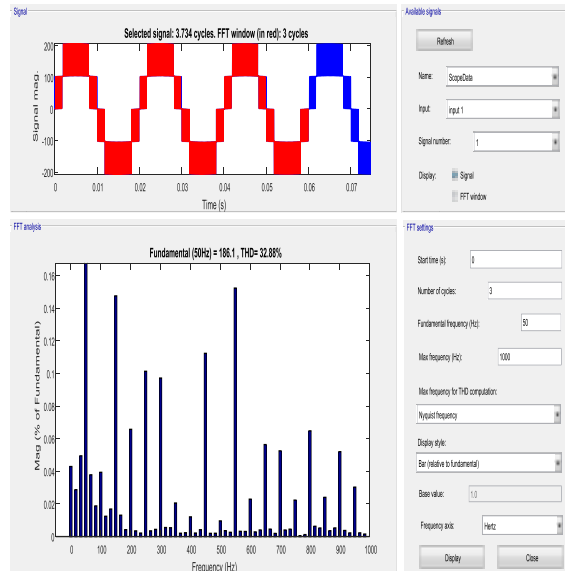


Figure 5: Voltage Output of a Single-Phase Seven-Level DCMLI on no load at $m=0.6$ for PD PWM

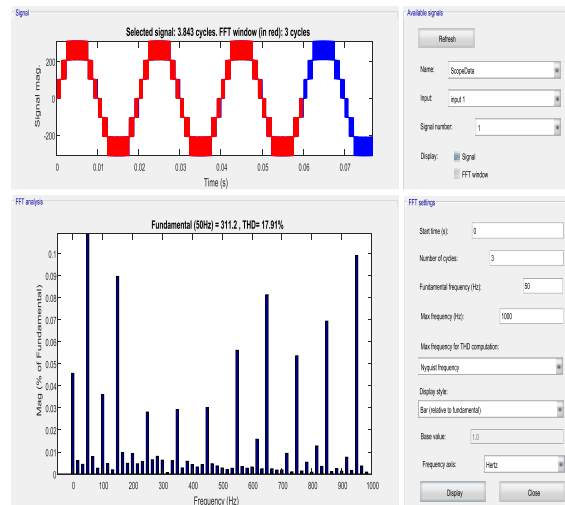


Figure 6: Voltage Output of a Single-Phase Seven-Level DCMLI on no load at $m=1.0$ for POD PWM

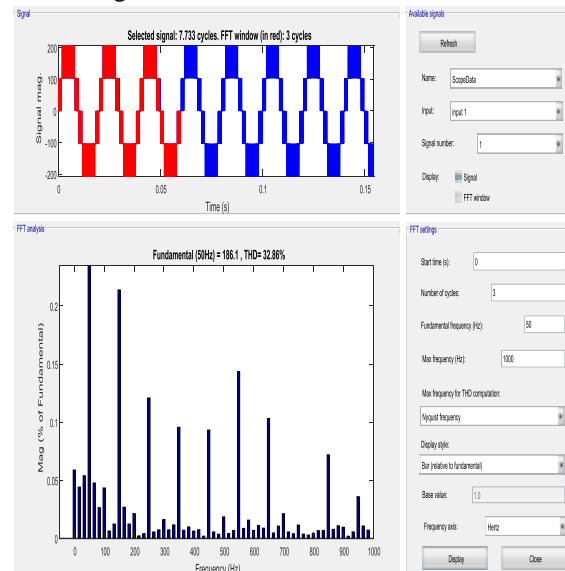


Figure 7: Voltage Output of a Single Phase Seven-Level DCMLI on no load at $m=0.6$ for POD PWM

4.1 THD simulation of the single phase seven level DCMLI for PD, and POD M.I = 0.6 to 1.0 using MATLAB/SIMULINK

The results analysis from frequency of PD, and POD are summarized in Table 2 to Table 4.

Table 2: THD and Fundamental magnitude of PD PWM technique of 7 level DC MLI

Modulation Index (M.I)	Fundamental Mag (50Hz)	RMS Values	Total Harmonic Distortion (THD) %
1	311.2	220.1	17.93
0.9	280.2	198.1	22.11
0.8	249.1	176.1	23.97
0.7	217.4	153.7	24.86
0.6	186.1	131.6	32.88

Table 3: THD and Fundamental magnitude of POD PWM technique of 7 level DC MLI

Modulation Index (M.I)	Fundamental Mag. (50 Hz)	Total Harmonic Distortion (THD) %
1	311.2 220.1	17.92
0.9	280.2 198.1	22.09
0.8	249.1 176.1	23.96
0.7	217.4 153.7	24.84
0.6	186.1 131.6	32.86

From Table 2 to Table 3, it shows that the modulation index of 1.0 has the lowest THD values of 17.93 % and 17.92 % respectively with fundamental frequency amplitudes of 311.2 for PD and POD SPWM in the FFT analysis of the single phase seven level DC MLI. From table 3, it shows that POD SPWM techniques have better THD performance than PD in a single phase seven level DCMLI due to low THD percentage recorded as 17.92 % with a magnitude of 311.2 over 3 cycles at a fundamental frequency of 50Hz over a maximum frequency of 1kHz.

V. CONCLUSION

Conclusively, the design and analysis a Single-phase Seven-level Diode Clamped MLI using POD SPWM technique has been achieved. The output of the inverter was observed to be 220.1V RMS with a THD of 17.92 % without filtering on no load which can be used at homes.

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