American Journal of Engineering Research (AJER)
e-ISSN: 2320-0847 p-ISSN : 2320-0936
Volume-8, Issue-10, pp-58-76
www.ajer.org
Research Paper Open Access

A Case Study of Return on Investment in Wafer-Ring Multi-sites Test Handler for the Semiconductor Industry Paper

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ABSTRACT : *With the increasing demand for high-complexity consumer Electronic products, the design of New Semiconductor chips needs to provide the required flexibility and speed. This trend shows that the functionality built into a single Semiconductor chip has continuously improved compared to the functionality 20 years ago. In contrast, Testing Costs in Semiconductor industries today can reach a substantial percent of the total Manufacturing Cost, thus affecting the Profit Margin. Numerous approaches have been introduced to lessen Testing Costs; one of them is the Multi-Site Testing. A case study was conducted to determine the effectiveness of Multi-site testing in reducing Testing Costs hence to improve the profit margin and improve the return on investment of the multi-sites test equipment's. To achieve the research goal, a Multi-Site Return on Investment (ROI) Model was developed using the test Cost Economic Model developed by Evan (1999) based on the economic theory of the firm, and by integrating important elements including economic Profit Margin and technology Multi-site efficiency. This model enabled the researcher to measure the capabilities of the Multi-site testing for the Cost of Test Deduction and it effectiveness in relation to improving the Profit Margin and the return on investment (ROI). The case study was conducted on Wafer-Ring Test-equipment setup. Five Multi-site configurations were configured. Testing time, indexing time, and Test yield-data were collected for the purpose of establishing the Testing Cost and calculating the Profit Margin. Five hypotheses were tendered to analyze the performance of the Test-equipment setup, including Multi-site versus Multi-site efficiency, Multi-site versus Testing throughput, Multi-site versus Testing Cost, Multi-site versus Profit Margin improvement and Multi-site versus ROI improvement. The findings were analyzed using one-way ANOVA, Post-hoc test. This research established that increasing the number of test sites is not sufficient to guarantee reduced Testing Cost while maintaining Profit Margin and improve of the ROI because, once the number of test sites increases correspondingly, the Testing time will increase as well. It is therefore proposed that future work be conducted on the Multi-Site Testing Approach together with other Testing Approaches that can reduce Testing time, such as concurrent Testing.*

KEYWORDS *Cost of Test, Testing economic model, Multi-sites testing, wafer-ring test handler, Return on Investment Model.*

Date of Submission: 30-09-2019 Date of acceptance: 15-10-2019

I. INTRODUCTION

Electronic devices, such as personal computers and cell phones, continue to reduce their selling price as a marketing strategy to maintain their position in the market and to stay competitive. For example, the Apple Macintosh with a speed of 8 MHz was launched in 1984 and sold for $1,995 USD to $2,495 USD (http://en.wikipedia.org/wiki/Macintosh; cited: 11 April 2012). The latest generation of the Macintosh family, the I-Mac 2.5 GHz to 3.1 GHz, which is approximately a thousand times faster than the original Macintosh, only sells at a price range of between $1,199 USD to $1,699 USD (http://store.apple.com/us/browse/home/shop_mac/family/imac/select; cited: 11 April 2016).

Although the speed of the Macintosh has increased 1000 times and more advanced features have been added to it, its price has decreased by approximately 47%. This example shows that products with high-performance semiconductor chips are not being sold at the price that people expected 20 years ago.

Companies are doing an excellent job of reducing fabrication cost by 25% to 30% (Goodall, 2002) over the past 50 years. Figure 1 shows that fabrication cost was predicted to decrease from 1 US cent per transistor in 1982 to 0.0001 US cent per transistor in 2012. However, the cost of testing has increased. In 2012, the cost of testing equaled the cost of fabrication (Bao, 2003).

Nowadays, fabrication cost is no longer the deciding factor for profit margin in the manufacture of semiconductor chips. Therefore, to reduce fabrication cost and the subsequent increase in testing cost, semiconductor manufacturers must continue to improve their "testing technology." Doing so will also allow them to stay competitive in the market. If the cost of testing is not reduced, the procedure will have a negative effect on the overall manufacturing cost of semiconductor chips in the future.

With the increasing demand for high-complexity consumer Electronic products, the design of New Semiconductor chips needs to provide the required flexibility and speed. This trend shows that the functionality built into a single Semiconductor chip has continuously improved compared to the functionality 20 years ago. In contrast, Testing Costs in Semiconductor industries today can reach a substantial percent of the total Manufacturing Cost, thus affecting the Profit Margin and the ROI in testing technologies.

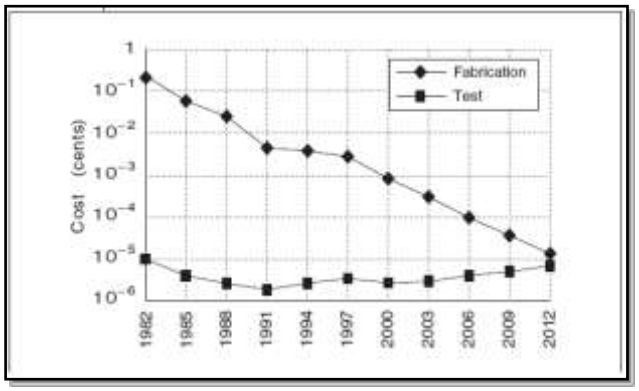


Fig.1. Cost of Testing a Transistor Approximates the Cost of Fabricating It (Bao G., 2003)

Numerous Approaches have been introduced to lessen Testing Costs; one of them is the Multi-Site Testing. A Case Study was conducted to determine the effectiveness of Multi-Site Testing in reducing Testing Costs which affecting the profit and the ROI. To achieve the research goal, a Multi-site ROI Model was developed based on the economic theory of the firm-Average Cost theory, by integrating important elements into the Model such as the technology Multi-site efficiency etc. Through the developed Model, this research managed to measure the capabilities of the Multi-site testing for the Cost of Test Deduction and the ROI measurement.

The case Studies were conducted on Wafer-ring Test-equipment. Five Multi-site configurations were configured on the Test-equipment setup for comparison. Testing time, indexing time, and Testing yield data were collected for the purpose of establishing the Testing Cost. The Hypothesis which was designed to analyze the performance of the Test-equipment setup is Multi-site versus Return on Investment. The hypothesis was analyzed using one-way ANOVA and Post-hoc test.

II. THE WAFER-RING HANDLER

The concept of the wafer-ring testing handling is similar to that of the lead frame strip testing. However, this handling method attaches the lead frame on top of the wafer ring. A photograph of the wafer-ring is shown in Figure 2. This testing method is used on lead-less packagers such as wafer-level packaging, ball-guided assembly, chip scale packaging, and so on.

Similar to lead frame strip-testing handling, the semiconductor chip is tested without singulating the chip from the leadframe. As shown in Figure 3 below, the process flow is basically similar to that of leadframe strip-testing handling, the only difference being the wafer ring, which is attached to the two leadframes, is transferred to the Test Area by pick-arm 1 and attached to the test chuck. The test chuck then transfers the wafer ring to the Test Area and, similar to the lead-frame testing handling, the wafer is punched to connect to the test socket/contactor. The test chuck moves in X and Y directions to test the entire chip on the wafer ring. The completely tested wafer ring is transferred to the output area by pick-arm 2. A photograph of the wafer ring test chuck is shown in Figure 4 below.

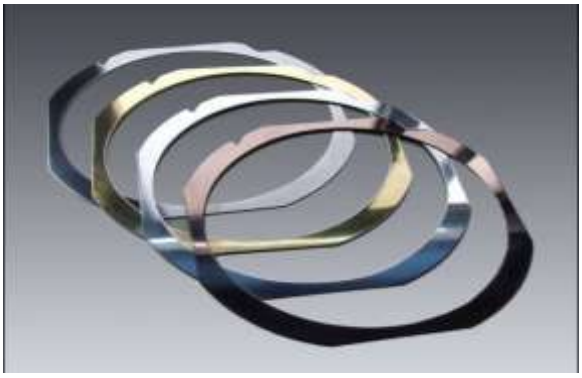


Fig.2. Example of Wafer Rings

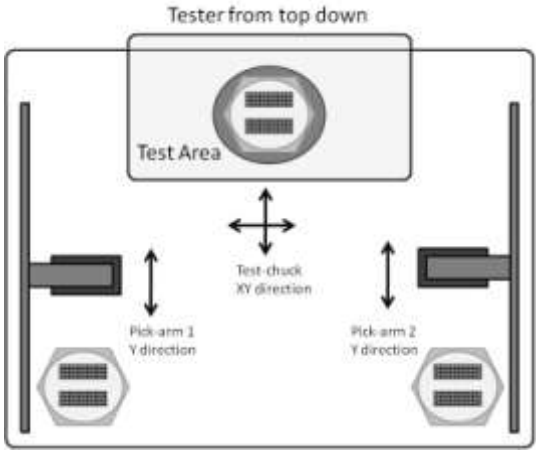


Fig.3. The Process Flow of the Wafer-Ring Testing-Handling Test Equipment

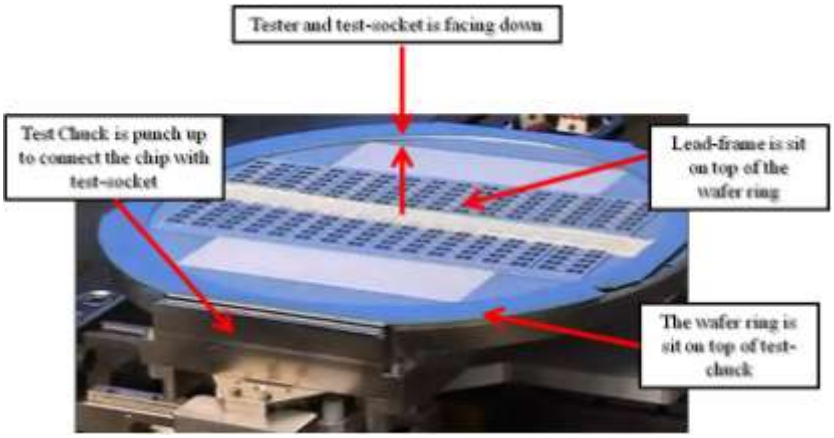


Fig.4. The Test Chuck of the Wafer-Ring Testing Handling

III. LITERATURE REVIEW

Trends in the ASP of semiconductor devices are moving in different directions; ASP had decreased by an average of 60.62% in the past 10 years (Aizcorbe, 2002). To overcome increasing manufacturing costs and decreasing ASP, the semiconductor industry has implemented several corrective actions to improve the fabrication or assembly process in the past 50 years. These measures include increasing the number of transistors built on a single chip (wafer size), improving production yields, and enhancing the overall equipment efficiency (Goodall, 2002). In implementing effective assembly cost reductions in the past, functional costs were reduced from 25% to 30% each year.

Since 2012, the fabrication or assembly cost is no longer the profit-margin deciding factor in setting the selling price of semiconductor chips; instead, it is the testing cost (NTRS, 1997). The reason behind this shift is the consistent growth of the number of transistors per semiconductor chip, which requires more testing resources (Goel, 2005). Furthermore, testing time is predicted to increase by 900% by 2014 relative to the year

1999, using conventional testing methods (Gonciari, 2002). As the testing process slows down, considerable test equipment is needed to produce the required Q because the ATE capital and interface expenditures are major cost drivers that comprise approximately 80% of the total testing expenditure. Therefore, reducing the testing cost is important in ensuring the competitiveness of a manufacturer in the semiconductor market. A number of corrective actions were implemented to reduce the testing cost, such as MS testing, RP testing, compression and design for testability method, built-in self-test function method, and concurrent tests.

To control and measure the testing cost in the semiconductor industry, various testing cost models have been formulated by considering current testing technologies. The models mainly use the ATC theory as reference. As mentioned, the ATC theory is implemented by dividing TC by the production output to calculate the cost involved in manufacturing a single product. From the literature review on testing cost models, testing yield and test equipment utilization are variables that affect TC. In addition, most of the current testing cost models calculate ATC as the main objective; however, these models disregard the profit margin in their calculation. The profit margin is the most important measurement in determining the capability of the test equipment setup. Thus, developing a new testing cost model that considers the profit margin with ATC is crucial.

Finally, the ROI basically refers to the overall performance degree which used to evaluate the efficiency of an investment or to compare the efficiency of a number of exclusive investments. ROI involves two main components, namely, the investment and the income or the so-called "earning." From the economic perspective, income or earning is the profit that has a direct relation with the revenue and cost. Investment has two types, namely, the autonomous investment and the induced investment.

IV. RESEARCH MODEL DEVELOPMENT

The models for the cost-of-test, cost-of-test profit margin, and ROI are illustrated in Figure 5. The figure shows that the model is developed through a stage-by-stage approach, starting from variable identification to the final derivation of the proposed models. A detailed discussion of each stage of the model development is provided in two subsections that cover the following steps:

- The development of the cost-of-test model based on average cost theory
- The development of the cost-of-test profit-margin model
- The development of the ROI test-technology model (ROITM)

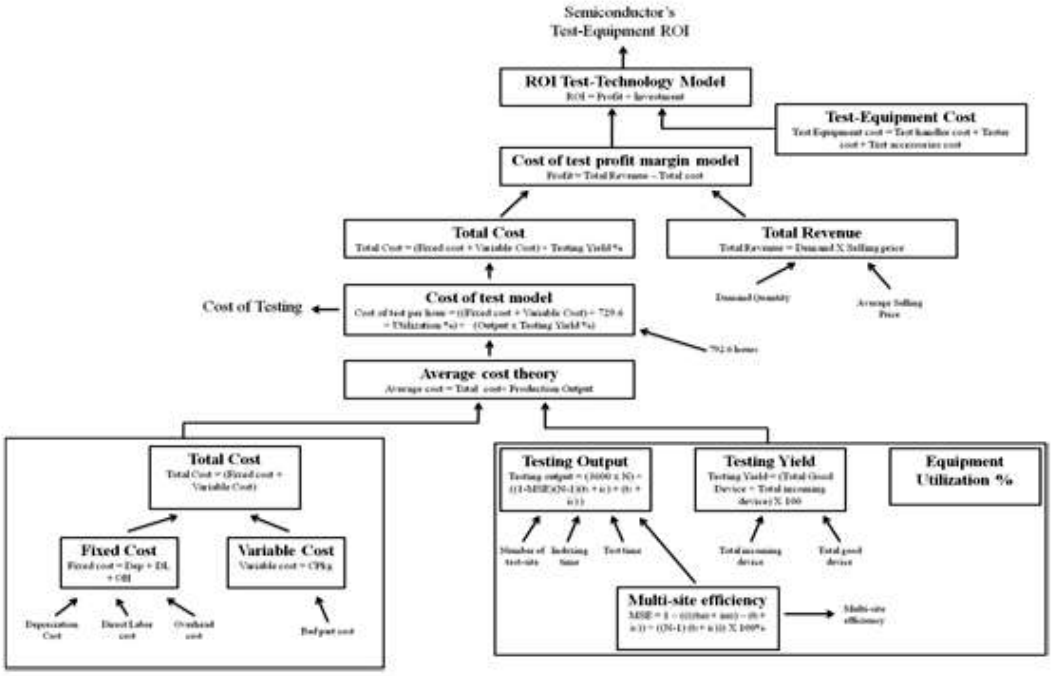


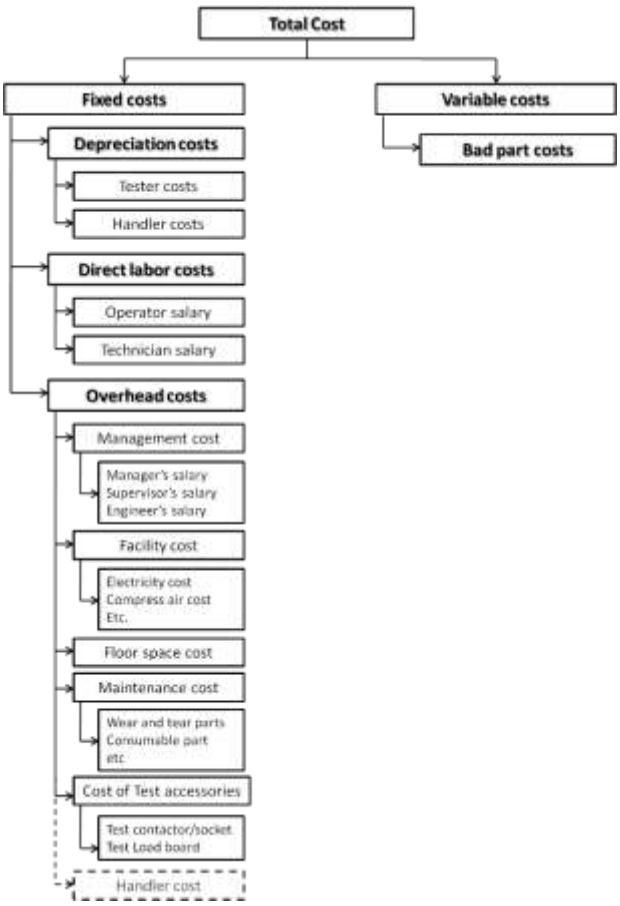
Fig.5. Cost of Test model, Profit margin model and ROITM

V. THEDEVELOPMENT OF THE COST OF TEST MODEL BASED ON AVERAGE COST THEORY

The cost-of-test model in this research was developed based on average cost theory, as shown in Equation 1. Average cost theory involves two elements: total cost and production output.

$$\text{Average Total Cost (ATC)} = \frac{\text{Total Cost (TC)}}{\text{Output (Q)}} \quad (1)$$

- **Total Cost -** According to the average total cost theory, the total cost included of fixed cost and the variable cost. For the multi-sites testing aspect, the variables which affected the total cost are shown in figure 6 as below.



Source: Author's own research

Fig 6. Multi-sites testing variables for total cost

- **Fixed Cost -** Whereby the fixed cost included of equipment depreciation cost (Dep) which contain of the tester cost and the test handler cost. Equation 2 was developed to calculate the equipment depreciation cost which span over five years from it purchase value to zero-cost.

$$\text{Dep} = \left(\frac{\text{Tester Cost} + \text{Handler Cost}}{5}\right) \div 12. \quad (2)$$

The second variable which affected the fixed cost is the direct labor cost (DL). The direct labor (DL) cost is the monthly salary of employees who directly contributes to the production output, such as operators and technicians. Direct labor cost is expressed in Equation 3:

$$\text{Direct Labor Cost per month} = \left(\text{Operator salary per month} \times 3\right) + \left(\text{Technician salary per month} \times 1.5\right) \quad (3)$$

For the operator variable, each test-equipment setup requires one operator, and thus, three operators are needed each day to cover three production shifts. For one shift, only one operator is required. To standardize the equation for ease of understanding, three shifts are used in this study.
For the technician variable, one technician can support two test-equipment setups. Therefore, only a half the cost is needed per test-equipment setup. To cover three production shifts, only 1.5 technicians are needed.
Operator and technician wages are based on a report published by JobStreet.com. (cited: 11 April 2012). In this study, the average wage is used as a reference for the aforementioned positions.
In addition, the **Overhead (OH)** cost is the cost incurred during production aside from equipment depreciation and direct labor costs. Overhead cost includes the following.

- **ManagementCost** - includes the monthly wages of the manager, supervisor, and engineer, which are considered as indirect labor costs. Wages data are based on a JobStreet.com report (cited: 11 April 2012). Equation 4 shows management cost calculation:

$$\text{Management cost} = \text{Manager's Salary} + \text{Supervisor's Salary} + \text{Engineer's Salary} \quad (4)$$

- **Facility Cost** is the monthly utility cost of electricity, compressed air, and so on.
- **Floor-Space Cost (FPS)** is the cost of the area occupied by the test-equipment setup. Equation 5 shows the calculation of floor space cost:

$$\text{FPS} = \left(\frac{\text{(Selling Price)}}{3000}\right) \text{X} \begin{matrix}\text{Test Equipment}\\ \text{floor space area}\\ \text{(Sq-Ft)}\end{matrix} \quad (5)$$

In this study, the calculation of floor-space cost is based on the Malaysian Government Valuation and Property Service Department Report 2011. The 2011 "Detached House Pricing" is adopted as a reference for calculating price per sq. ft. Test equipment setup floor space costs are then calculated as the X number of area sq. ft. needed multiplied by the per sq. ft. pricing, as shown in Equation 5.

- **Maintenance Cost** is the cost spent in one month to maintain the test equipment, such as wear-and-tear part cost, consumable part cost, and so on. The study estimates maintenance cost at 5% per year of the test equipment cost.
- **Cost-of-Test Accessories** includes the test contactor and load board, which are described as follows:

i. Load Board/Probe Card is the electronic printed circuit board used for interfacing between the tester and the test handler.
ii. Test Contact Socket is the mechanism used to connect the semiconductor device to the load board.

- **Variable Cost**

Another factor identified as part of the total cost calculation that has an effect on the test yield is the variable cost. From the research point of view, the variable cost is categorized as a changeable cost because it is not fixed, and it will change when the testing yield is modified.

The variable cost that needs to be included is the bad-part cost based on the test cost model developed by Rivoire (2003). The bad-part cost is imperative in this research, particularly when dealing with multi-site configurations, because the developed model will be validated using this configuration. When changes are implemented during testing, they may affect the consistency of the testing yield, which depends on multi-site repeatability efficiency.

To include the bad-part cost into the total cost equation, an equation has to be derived to calculate the cost of bad parts. The first step in deriving the bad-part cost equation is to imply the appropriate equation that can calculate the quantity of bad parts. Equation 6 is derived for this purpose.

$$\text{Number of bad part} = \text{Total Input X } \left[100\% - (\text{Testing Yield})\right] \quad (6)$$

Based on Equation 6, total incoming chip quantity is multiplied by the bad part yield, which can be obtained by deducting the testing yield from 100%. The testing yield is the tested good part percentage that can be obtained from Equation 7:

$$\text{Testing yield \%} = \left(\frac{\text{Total Good Device}}{\text{Total Incoming Device}} \text{ X } 100 \right) \quad (7)$$

Finally, to calculate the cost of the tested bad parts, the ASP of a particular type of semiconductor chip is multiplied with the number of bad parts obtained from Equation 6. Therefore, Equation 8 is derived to determine the total cost of tested parts.

$$C_{Pkg} = \text{ASP}\left[\text{Total Input X}\left[\text{ Bad part \% }\right]\right] \quad (8)$$

where:
i. CPKg is the cost of bad parts;
ii. ASP is the average selling price;
iii. Total Input is the total input of semiconductor chips; and
iv. Bad Part % is the tested bad chips obtained by deducting the testing yield from 100%.

All costs have been discussed thoroughly to facilitate total cost calculation. Therefore, by putting together all the equations, Equation 9 is derived to demonstrate how the total cost has been integrated:

$$\text{Total Cost} = \text{Dep} + \text{DL} + \text{OH} + C_{Pkg} \quad (9)$$

Another element incorporated in average cost theory for the developed model is production output. A detailed discussion of this element is provided in the following subsection:-

- **Production Output**

Production output consists of three fundamentals: testing output (throughput), testing yield, and the equipment utilization percentage. Detailed explanations for these fundamentals are as follows.

$$UPH_{good} = \frac{3600 \text{ X N}}{((1\text{-MSE})(N\text{-}1)(t_I+i_I) + (t_I+i_I))} \text{ X } \left(\frac{\text{Total Good Device}}{\text{Total Incoming Device}} \text{ X } 100 \right) \quad (10)$$

Equation 10 was developed to calculate the production throughput whereby the throughput obtained is the tested good product by take into account the testing yield whereby the testing yield mean that the percentage of tested good. The equation of testing yield % is shown in equation 7 in this paper.

The equation 10 was integrated with the Multi-sites efficiency (MSE) as well so that the comparison between the multi-sites versus the multi-sites efficiency (MSE) can be obtained, but in this paper, will not analyze of this hypothesis and will reserve for next paper publication.

To integrate the MSE into the equation, the throughput equation from Evans (1999) as shown in equation 11 need to further enhance. Following discuss step by step on how the MSE was integrated into the throughput equation.

$$UPH_{insertions} = \frac{3600 \text{ x } n}{t_{ms} + i_{ms}} \quad (11)$$

where:
i. tms is the multi-site test time, that is, the time spent to complete the testing of a semiconductor chip.
ii. ims is the multi-site indexing time, that is, the semiconductor chip exchange time within the tested chip replaced with a new untested chip.
iii. n is the number of test sites, that is, the number of semiconductor chips tested in a single contact.

To achieve the integration with the MSE, the throughput equation developed by Evans (1999), shown as Equation 11, is enhanced by integrating the MSE model developed by Kelly (2008). The MSE proposed by Kelly is presented as Equation 12:

$$MSE = \left(1 - \frac{\Delta t}{\Delta N(t_1)}\right).100\% \qquad (12)$$

where:

i. Δt is the change in testing time between single-site and multi-site testing; and
ii. ΔN is the number of different test sites between single-site and multi-site testing.

Equation 12 is further derived, as shown in Equation 13.

$$MSE = \left(1 - \frac{(t_{MS} - t_1)}{(N-1)(t_1)}\right).100\% \qquad (13)$$

where:

i. tMS is the multi-site test time, and t1 is the single-site test time; and
ii. N is the number of test sites for multi-site testing.

The test handler affects testing throughput. Therefore, the test handler indexing time has to be included as part of the MSE equation. In doing so, Equation 14 is derived by including the indexing time (i), as follows:

$$MSE = 1 - \left(\frac{((t_{MS}+i_{MS}) - (t_1+i_1))}{(N-1)(t_1+i_1)}\right).100\% \qquad (14)$$

For the integration of the equations to work, one must have prior understanding of the relationship between the throughputs and MSE. To determine the relationship between MSE and multi-site, the variables of MSE, which is related to the throughput, need to be understood. Equation 11 and Equation 14 show that the multi-site test time (tms) and multi-site indexing time (ims) are common variables in both equations.

In Equation 14, tMS and iMS represent multi-site test time and indexing time. Therefore, to clearly derive the relationship between tms and ims in relation to MSE, the integration process shown in Figure 7 is carried out.

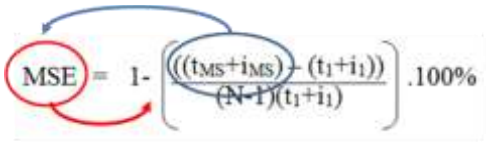


Fig.7. Deriving the Relationship between t_{ms} and i_{ms} with MSE

As Figure 3 illustrates, tms and ims move to the left side of the equation, whereas MSE moves to the right side. The final computation for the equation of tms and ims in relation to MSE is derived and shown in Equation 15.

$$(t_{MS} + i_{MS}) = (1\text{-}MSE)(N\text{-}1)(t_1+i_1) + (t_1+i_1). \qquad (15)$$

Finally, Equation 15 is integrated into Equation 11 to obtain the computation for testing throughput, which includes MSE as part of the calculation. Figure 8 below shows the computation of the integration, and the complete integration is illustrated in Equation 16:

$$UPH_{insertions} = \frac{3600 \times n}{(1\text{-}MSE)(N\text{-}1)(t_1+i_1) + (t_1+i_1)}$$

Fig.8. The Computation of the Integration of Equation 15 into Equation 11

where:

i. UPHinsertions are represented by the testing output in one hour.

- **Equipment Utilization (U)**

Equipment utilization percentage refers to the percentage by which the test equipment is used in producing output. When the test equipment is 100% utilized, then no cost is lost. The aforementioned cost refers to the total cost, as indicated in Equation 9. When equipment utilization achieves a higher percentage, the cost becomes cheaper. By contrast, when utilization percentage begins to decrease, then the cost increases (Horgan, 2004).

Given that equipment utilization percentage affects the total cost, then the former must be included in Equation 9. Therefore, the total cost equation, which involves equipment utilization percentage, is depicted in Equation 17.

$$\text{Total Cost per month} = \frac{(\text{Dep} + \text{DL} + \text{OH} + C_{Pkg})}{U} \quad (17)$$

The total cost obtained from Equation 17 is the monthly testing expenditure. However, the testing throughput is calculated based on the hourly production output. Therefore, to obtain the total cost per hour, Equation 17 has to be further derived, as shown in Equation 18.

$$\text{Total Cost per hour} = \frac{\left(\frac{\text{Dep} + \text{DL} + \text{OH} + C_{Pkg}}{729.6}\right)}{U} \quad (18)$$

Where the total cost is divided by 729.6 to obtain the hourly cost; and 729.6 is the total number of production hours in one month.

After all the equations and variables for average cost theory are defined, the next step is to integrate all the equations into average cost theory to derive the cost of the model. The integration is illustrated in Figure 9:

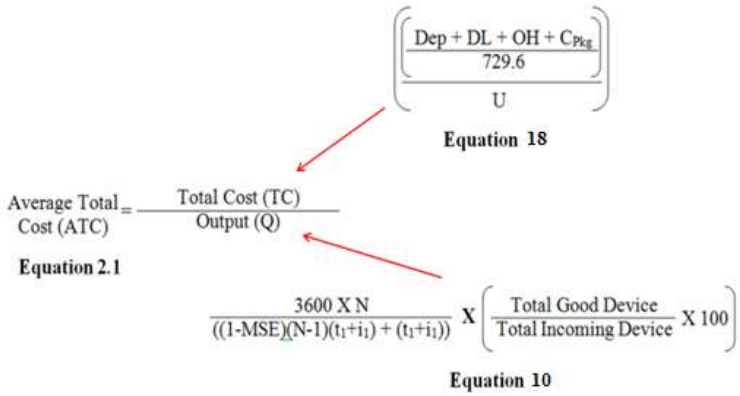


Fig.9. The Integration of Equations 18 and 10 into Equation 1.

As shown in Figure 5, the average cost in Equation 1 is integrated with Equation 18, which is the total cost in one hour, and Equation 10, which is the total number of good chips tested in one hour.

The final cost of test model is then integrated, as shown in Equation 19:

$$CPU_{GOOD} = \frac{\left(\frac{\left(\frac{\text{Dep} + \text{DL} + \text{OH} + \text{CPkg}}{729.6}\right)}{U}\right)}{\left(\frac{3600 \text{ X N}}{((1-\text{MSE})(N-1)(t_1+i_1) + (t_1+i_1))}\right) \text{X} \left(\frac{\text{Total Good Device}}{\text{Total Incoming Device}} \text{ X } 100\right)} \quad (19)$$

Where

i. CPUGOOD is the cost per good unit in one hour.
ii. Dep is the depreciation cost per month of the test equipment.
iii. DL is the direct labor cost per month.
iv. OH is the overhead cost per month.
v. CPKg is the bad-unit cost.
vi. N is the number of test sites.
vii. t is the test time.
viii. i is the indexing time.

ix. 729.6 is the number of hours per month.
x. U is the test-equipment utility percentage per hour.

After successfully deriving the new cost-of-test model, as shown in Equation 19, the second equation that must be developed is the cost-of-test profit-margin model. Before developing this model, the relationship between the profit and cost of test must be established so that the variables for the cost of test, which is related to profit, can be integrated into the model. As Samuelson (2001) asserts, profit can be obtained by deducting the total cost from the total revenue. A detailed discussion of the cost-of-test profit-margin model is provided below.

As shown in Figure 5, two elements inclusive of the total cost and the total revenue are incorporated in the profit calculation. The total cost can be obtained from the Equation 19 (cost-of-test model). In this section, the derivation of the total revenue is discussed which is divided into three subsections to clearly explain the profit-margin model. The first subsection explains the derivation of the total cost from Equation 19. Follow by the discussion of the total revenue derivation and finally the last subsection is discussing the development process of the cost-of-test profit-margin model.

- **Total Cost Derived from Equation 19**

The total cost is part of the average cost as indicated in Equation 1, therefore the average cost equation is used to derive the relationship between the total cost with the cost of test due to the cost-of-test equation was derived from average cost theory. The derivation process is shown in Figure 10.

Source: Author's own study

Fig.10. Deriving the Total Cost through the Equation of the Average Cost.

To derive the total cost equation through average cost theory as shown in Figure 10, the output (Q) is transfer from the left side of the equation to its right side, and the dividend becomes the multiplier. By then the total cost formula in relation to the average cost theory which is derived as shown in Equation 20 as follow:

$$\text{Total Cost} = \text{Average Total Cost} \times \text{Output} \tag{20}$$

Due the cost of test model was derived from the average cost theory; therefore, Equation 20 is further derived and expressed as Equation 21.

$$\text{Total Cost} = \text{Cost of Test} \times \text{Output} \tag{21}$$

As shown in equation 21 as above, the total cost is equal to the cost of test multiplied by the production output (Testing throughput). Therefore, to derived the total cost, the variables in Equations 19 and 16 are integrated with Equation 21, as illustrated in Figure 11, and the final equation is shown in Equation 22.

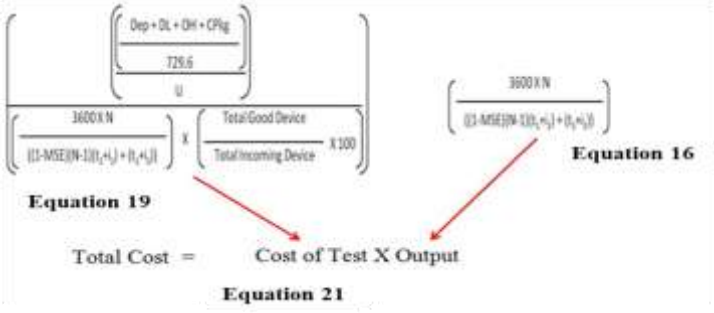


Fig.11. Integration of Equations 19 and 16 into Equation 21.

$$\text{Total Cost} = \frac{\left(\frac{\left(\frac{\text{Dep} + \text{DL} + \text{OH} + \text{CPkg}}{729.6}\right)}{\text{U}}\right)}{\left(\frac{3600 \times \text{N}}{((1-\text{MSE})(\text{N}-1)(t_1+i_1)+(t_1+i_1))}\right) \times \left(\frac{\text{Total Good Device}}{\text{Total Incoming Device}} \times 100\right)} \times \left(\frac{3600 \times \text{N}}{((1-\text{MSE})(\text{N}-1)(t_1+i_1)+(t_1+i_1))}\right) \quad (22)$$

Equation 22 is further simplified by canceling the unit per hour (UPHinsertion) equation, as shown in Equation 23.

$$\text{Total Cost} = \frac{\left(\frac{\left(\frac{\text{Dep} + \text{DL} + \text{OH} + \text{CPkg}}{729.6}\right)}{\text{U}}\right)}{\left(\frac{3600 \times \text{N}}{((1-\text{MSE})(\text{N}-1)(t_1+i_1)+(t_1+i_1))}\right) \times \left(\frac{\text{Total Good Device}}{\text{Total Incoming Device}} \times 100\right)} \times \left(\frac{3600 \times \text{N}}{((1-\text{MSE})(\text{N}-1)(t_1+i_1)+(t_1+i_1))}\right) \quad (23)$$

The final derivation of the total cost calculation is shown in Equation 24.

$$\text{Total Cost} = \frac{\left(\frac{\left(\frac{\text{Dep} + \text{DL} + \text{OH} + \text{CPkg}}{729.6}\right)}{\text{U}}\right)}{\left(\frac{\text{Total Good Device}}{\text{Total Incoming Device}} \times 100\right)} \quad (24)$$

As indicated in Equation 24 show that the equipment utilization percentage and good-unit yield influence the total cost. After obtained the total cost equation 24, total revenue theory is discussed in the following section.

- **Total Revenue**

According to McKenzie (2006) the total revenue is equal to market demand multiplied by product average selling price as expressed in Equation 25.

$$\text{Total Revenue} = \text{Demand} \times \text{Selling Price} \quad (25)$$

Demand is the number of semiconductor chips as required by the market, and selling price refers to the average selling price (ASP) for a particular semiconductor chip. For this research, the hourly test throughput is used as the quantity of demand to facilitate the calculation.

The two factors that influence profit are discussed. The following section elucidates the development process of the cost-of-test profit-margin model.

- **Development Process of the Cost-of-Test Profit-Margin Model**

Profit is equal to the total cost minus the total revenue (Kingma, 2010) as expressed in Equation 26 as below

$$\text{Profit} = \text{Total Revenue (TR)} - \text{Total Cost} \quad (26)$$

Equation 26 shows that two elements affect profit: total revenue and total cost.

Equations 24 and 2.5 are integrated into Equation 26, as shown in Figure 12 to develop the final test profit-margin model as shown in Equation 27.

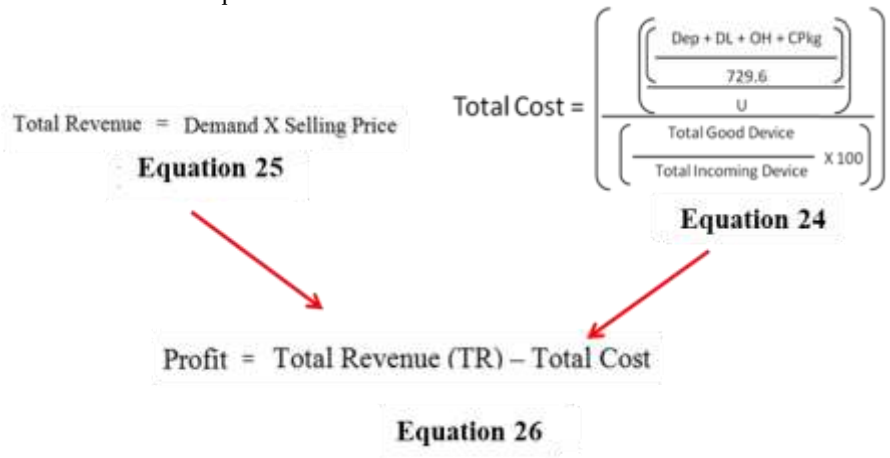


Fig.12. Integration of Equations 24 and 25 into Equation 26.

$$\text{Profit} = \left[\text{Demand X Selling Price}\right] - \left[\frac{\left(\frac{\text{Dep + DL + OH + CPkg}}{729.6}\right)}{\text{U}} \Big/ \left(\frac{\text{Total Good Device}}{\text{Total Incoming Device}} \text{ X } 100\right)\right] \quad (27)$$

The successfully developed of the test-profit margin model as shown in Equation 27 enabling the calculation of the cost-of-test profit margin for the research hypotheses.

Changing of the demand and test-equipment throughput to produce the required demand affects the test-equipment utilization percentage which affecting the number of the test equipment to produce that demand. Therefore, Equation 27 must be further improved to solve this problem. The following section is discussing the development of the equations which take into consideration of the utilization percentage and the change in the number of test equipment when the required demand is changed.

- **Equipment Utilization Percentage Based on Test Output**

To simulate different production outputs or required demands, then the Calculation of the equipment utilization percentage according to the test output increment across different test-site setups is necessary.

As indicated, the equipment utilization percentage and good-unit yield is affecting the total cost. Therefore, by using Equation 28 the equipment utilization percentage for different test throughputs can be obtained.

$$\text{U\% for Production Output (U\%O)} = \frac{\text{Production Output}}{\text{UPH}_{\text{insertion}}\text{ (Perfect Condition)}} \times 100, \quad (28)$$

Where

i. Production output or the required market demand is divided by $\text{UPH}_{\text{insetion}}$ in a perfect condition.

$UPH_{insertion}$ in a perfect condition refer to the maximum test throughput that the test equipment can produce via 100% MSE in one hour which can be obtained with Equation 16.

However, when test equipment is 100% utilized, additional test equipment is required to produce an additional test throughput therefore Equation 16 cannot result in an accurate calculation. The utilization percentage equation in Equation 28 need to further enhanced to solve this problem, as shown in Equation 29.

$$\text{Actual U\% for Production Output (AU\%O)} = \frac{\text{U\%O}}{\text{Number of Test Equipment}} \quad (29)$$

where the AU%O or actual utilization percentage can be calculated by dividing the U%O with the number of required test-equipment setups to produce the required test output. Hence, the actual utilization percentage per test-equipment setup can be calculated accurately.

As indicated, when the test equipment is 100% utilized then additional test equipment is required to produce the additional test output whereby the increment in the number of test equipment depends on the required output and the utilization percentage.

- **Cost of Good Unit Calculation Based on the Increment in Output Demand**

The AU%O and the required NOTE is integrated into the total cost equation as indicate in Equation 24 to obtain the cost of good unit based on the increment in test output demand. The integration shown in Figure 13 and the new total cost equation which is taking into account the AU%O and NOTE are derived in Equation 30 as below:

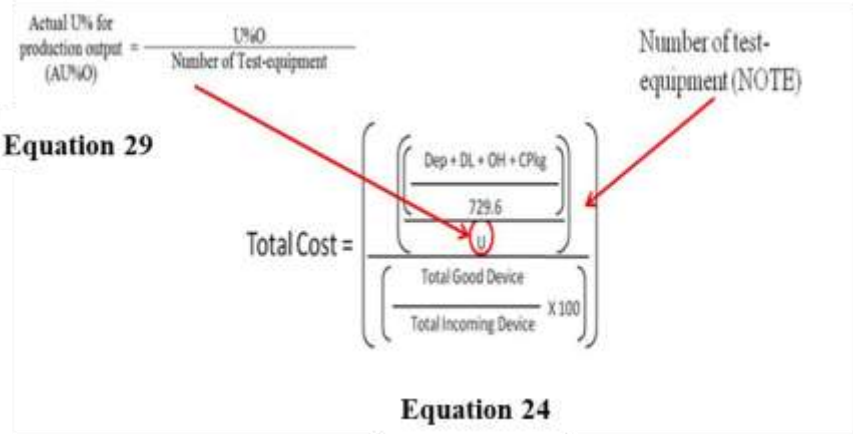


Fig.13. Integration of Actual Utilization Percentage and NOTE into Equation 24

$$\text{Total Cost} = \frac{\left(\left(\frac{\text{Dep + DL + OH + CPkg}}{729.6}\right) \text{X NOTE}\right)}{\left(\frac{\text{Total Good Device}}{\text{Total Incoming Device}} \text{ X 100}\right)} \quad (30)$$

where NOTE is the number of test-equipment setups required for a particular production output, and the utilization percentage (U) is replaced with the actual utilization percentage based on the required output (AU%O).

Finally, the profit-margin equation which includes AU%O and NOTE is successfully developed which is shown in Equation 31.

$$\text{Profit} = \left(\text{Demand X Selling Price}\right) - \left(\frac{\left(\frac{\left(\frac{\text{Dep + DL + OH + Cm}_E}{729.6}\right)}{\text{AU\%O}}\right) \text{X NOTE}}{\left(\frac{\text{Total Good Device}}{\text{Total Incoming Device}} \text{ X 100}\right)}\right) \quad (31)$$

- **Development of the ROI Test-Technology Model (ROITM)**

To develop ROITM, the relation of ROI with cost and profit must be identified. The computation of ROI is conducted by dividing the net income with the investment (Thamhain, 2005). The equation is derived in Equation 2.23.

$$\text{ROI} = \frac{\text{Revenue (R)} - \text{Cost (C)}}{\text{Investment (I)}} \quad (32)$$

Equation 32 shows that the net income is the revenue minus the cost, which is the equation of profit, as shown in Equation 26.

$$\text{Profit} = \text{Total Revenue (TR)} - \text{Total Cost} \quad (26)$$

The profit model developed for the semiconductor testing technology is shown in Equation 31. The integration of Equation 31 into Equation 32 is required to develop ROITM, as shown in Figure 14.

$$\left(\text{Demand X Selling Price}\right) - \left(\frac{\left(\frac{\left(\frac{\text{Dep + DL + OH + Cm}_E}{729.6}\right)}{\text{AU\%O}}\right) \text{X NOTE}}{\left(\frac{\text{Total Good Device}}{\text{Total Incoming Device}} \text{ X 100}\right)}\right) \quad \textbf{Equation 31}$$

$$\text{ROI} = \frac{\text{Revenue (R)} - \text{Cost (C)}}{\text{Investment (I)}} \quad \textbf{Equation 32}$$

Fig.14. Integration of Equation 31 into the ROI model (Equation 32)

The investment in this research is the investment of multi-site test-equipment cost and the related operation cost, which is the total cost, as shown in Equation 30. The investment equation is shown in Equation 33.

$$\text{Investment} = \quad \text{Total Cost} = \left(\frac{\left(\frac{\left(\frac{\text{Dep} + \text{DL} + \text{OH} + \text{CPkg}}{729.6} \right)}{\text{AU\%O}} \right) \text{X NOTE}}{\left(\frac{\text{Total Good Device}}{\text{Total Incoming Device}} \text{ X 100} \right)} \right) \quad (33)$$

The final ROITM model computation is shown in Equation 34.

$$\text{ROI} = \frac{\left(\text{Demand X Selling Price} - \left(\frac{\left(\frac{\left(\frac{\text{Dep} + \text{DL} + \text{OH} + \text{CPkg}}{729.6} \right)}{\text{AU\%O}} \right) \text{X NOTE}}{\left(\frac{\text{Total Good Device}}{\text{Total Incoming Device}} \text{ X 100} \right)} \right) \right)}{\left(\frac{\left(\frac{\left(\frac{\text{Dep} + \text{DL} + \text{OH} + \text{CPkg}}{729.6} \right)}{\text{AU\%O}} \right) \text{X NOTE}}{\left(\frac{\text{Total Good Device}}{\text{Total Incoming Device}} \text{ X 100} \right)} \right)} \quad (34)$$

VI. RESULTS

Table 1 shows two perspectives of the ROI in multi-site testing for wafer-ring test equipment. When the utilization is low, the ROI rate is also low; when the utilization rate reaches the maximum throughput of the test equipment, the ROI rate is also maximized. For example, for the single-site testing that produces 1,000 UPH, which is 30% of the maximum throughput capability of 3,365 UPH, only 9.628% of the ROI rate is achieved. When the test equipment produces 2,000 UPH, which is 59% of the test equipment utilization, 41.551% of the ROI rate can be achieved. The ROI rate is increased to 94.741% to produce 3,000 UPH, which is 89% of the maximum utilization. However, the ROI rate drops to 41.551% to produce 4,000 UPH because the test-equipment setup increases to two. The first test equipment achieves 100% utilization, whereas the second test equipment achieves only 19% utilization. The unutilized rate of 81% is wasted. The second perspective shown by the data is the multi-site factors of the ROI rate. The ROI average rate changes when the test site changes, but the data do not reflect the increment in test-sites to guarantee the improvement in the ROI rate. Table 4.30 shows that X32 sites have a lower rate than quad, octal, and X16 sites because of the investment of X32 sites, which is the highest among the test-site setups. Nevertheless, the expected throughput improvement is not provided, as shown in Figure 15.

Table1. Summary of the ROIMT Rate for Wafer-Ring Test Equipment

ROI					
Output	Single site	Quad sites	Octal sites	X16 sites	X32 sites
1,000	9.638%	6.648%	6.408%	6.134%	6.261%
2,000	41.551%	29.590%	28.631%	27.535%	28.045%
3,000	94.741%	67.828%	65.670%	63.204%	64.351%
4,000	41.551%	121.361%	117.525%	113.141%	115.179%
5,000	65.487%	46.797%	45.299%	43.586%	44.383%
6,000	94.741%	67.828%	65.670%	63.204%	64.351%
7,000	56.917%	92.683%	89.746%	86.389%	87.950%

8,000	74.647%	121.361%	117.525%	113.141%	115.179%
9,000	94.741%	153.863%	149.008%	143.460%	64.351%
10,000	117.199%	83.973%	81.309%	78.265%	79.680%
11,000	79.449%	101.817%	98.594%	94.910%	96.623%
12,000	94.741%	121.361%	117.525%	113.141%	115.179%
13,000	111.362%	142.604%	138.102%	132.957%	135.349%
14,000	82.401%	92.683%	160.325%	154.359%	87.950%
15,000	94.741%	106.544%	103.172%	99.319%	101.111%
16,000	107.932%	121.361%	117.525%	113.141%	115.179%
17,000	84.398%	137.134%	132.803%	127.855%	130.156%
18,000	94.741%	153.863%	149.008%	143.460%	93.105%
19,000	105.674%	109.431%	105.969%	102.012%	103.852%
20,000	117.199%	121.361%	117.525%	113.141%	115.179%
21,000	94.741%	133.903%	129.674%	124.841%	127.088%
22,000	104.076%	147.057%	142.415%	137.111%	96.623%
23,000	113.846%	160.822%	155.749%	149.952%	105.699%
ROI Average					
276,000	Single site	Quad sites	Octal sites	X16 sites	X32 sites
	85.94%	106.17%	105.88%	101.92%	90.99%

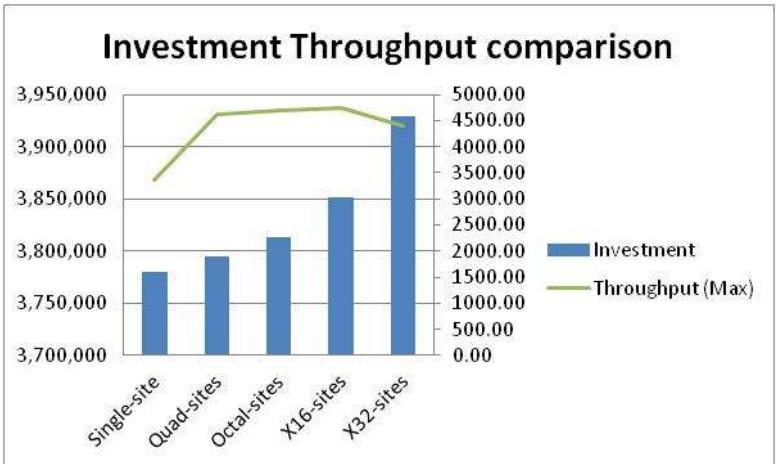


Fig.15. Comparison of Investment and Throughput

Table2. ROIMT Verification of the Wafer-Ring Test Equipment

ROITM			
	New model	**Evans's Model**	**Error %**
Single site	85.94%	35.0200%	59.25%
Quad sites	106.17%	25.0026%	76.45%
Octal sites	105.88%	29.7650%	71.89%
X16 sites	101.92%	23.6433%	76.80%
X32 sites	90.99%	24.5742%	72.99%
		Average Error %	71.48%

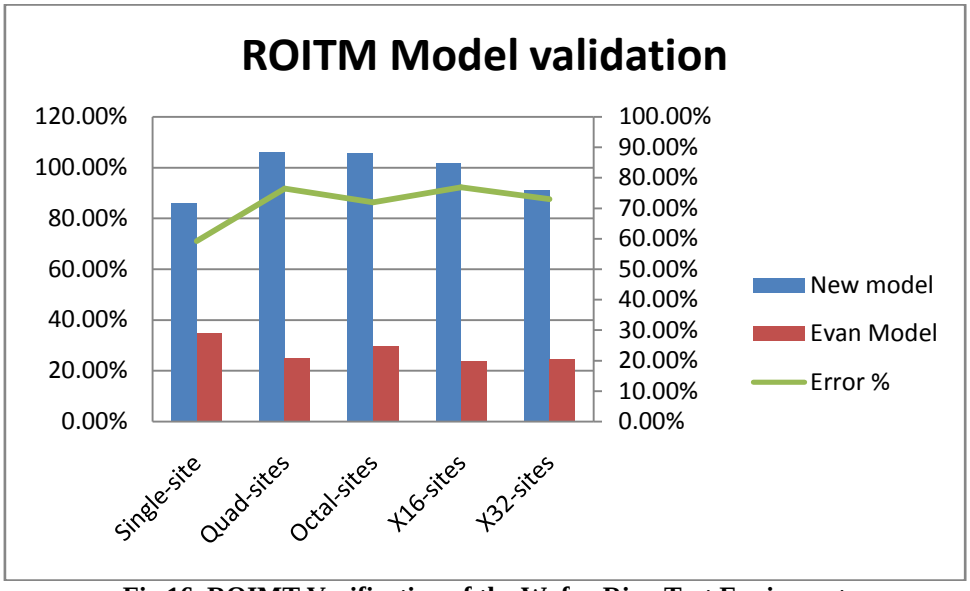


Fig.16. ROIMT Verification of the Wafer-Ring Test Equipment

As shown in Table 2 and Figure 16, as in Case Study, Evans's cost model is integrated to the ROI model to compare with the ROITM that is mainly developed for this research. Evans's model does not include the test handler and MSE as part of the calculation, which provides an inaccurate outcome for ROI study. Table 5.31 shows error differences between ROITM and Evans's model. Errors of 59.25%, 76.45%, 71.89%, 76.8%, and 72.99% are found in the test-equipment setups of single, quad, octal, X-16, and X-32 sites provided by the two models, respectively. In summary, an average error of 71.48% is generated between the two models. The verification in Case Study 2 successfully proves the difference between the new model and Evans's model.

In summary, the cost of testing and profit are affected by the total cost and production output. The handler cost is one of the major factors that affect the cost calculations. Thus, the correction accomplished by transferring the test-handler cost from the overhead cost to the equipment-depreciation cost has a significant effect on the accuracy of the cost calculation.

The production output is affected by the test throughput and test yield because the test throughput is affected by MSE. When MSE increases, the test throughput also increases.

MSE is affected by the test time, indexing time, and test-site configuration. The test time must be kept low when the test site increases the indexing time to achieve better MSE. MSE decreases when the indexing and test times increase in parallel with the increase in the number of test sites.

Two factors affect ROITM. The first factor is the utilization percentage. When the utilization is low, the ROI rate is also low; when the utilization rate reaches the maximum throughput of the test equipment, the ROI rate is also maximized. The second factor is the multi-site factors on the ROI rate. The ROI average rate changes when test site changes, but the data do not reflect the increment in test-sites to guarantee the improvement in ROI rate. The improvement depends on the comparison between the throughput and the investment on the multi-site test technology. If the investment does not produce the expected throughput, then a low ROI rate is generated.

From the case studies, the cost of test can be reduced and the profit margin can be increased in two ways: either by reducing the total cost or increasing the production output. A discussion of the scenarios is provided below.

Scenario 1: The average cost is low when the total cost is decreased and the production output remains the same.
Scenario 2: The average cost is low when the total cost remains the same but the production output increases.
Scenario 3: The average cost significantly decreases when the total cost decreases and the production output increases.

The ideal scenario to reduce the cost of test is 3. In practice, however, this scenario is difficult to achieve because additional test accessories, such as test contactors, are needed to increase the production output, and additional equipment increases total costs.The perspective of ROITM can also be summarized in the following three scenarios:

Scenario 1:A high utilization rate contributes to a high ROI rate.
Scenario 2: The investment in multi-site test equipment that contributes to significant throughput improvement increases the ROI rate.
Scenario 3: The investment in multi-site test equipment that does not contribute to significant throughput improvement will not having the lower ROI rate.
In this section, the cost-of-test model, cost-of-test profit-margin model, and ROITM are successfully validated. The following section discusses the multi-site analysis for the case study.

- **Hypothesis: Multi-Site versus ROIMT Improvement**

The analysis was used the alpha level of 0.05. As indicated, five independent levels of configurations (a) are selected: single, quad, octal, X16, and X32 sites. Each level contains 30 data sets (n). In this case, the following data are determined:
a = 5 independent levels,
n = 30 sets of data, and
N = 150.
Therefore, the degrees of freedom are calculated as
dfBetween= 5 −1 = 4,
dfWithin = 150 − 5 = 145,
dfTotal= 150 − 1 = 149.

From the degrees of freedom between and within, which is (4,145), refer to the F-Table, with the obtained critical value at 2.3719. Therefore, if the F-value is smaller than the critical value, then the null hypothesis is accepted; otherwise, the null hypothesis is rejected.

Refer to Table 1 for the wafer-ring test-equipment ROI summary of the production output simulation from 1,000 to 23,000. The analysis for the hypothesis is provided in the following sections.

- **Analysis of Hypothesis**

The hypothesis for the ROI analysis is as follows.
H0: An improvement in the test site has no effect on the improvement in ROI.
H1: An improvement in the test site has an effect on the improvement in ROI.

Table3. ANOVA Results for ROI

ANOVA Table

	SS	df	MS	F
Between	31.69	4.00	7.92	1.43
Within	610.70	110.00	5.55	
Total	642.38	114.00	5.63	

Table3 shows that the F-value is 1.43, which is lower than the critical value of 2.4542. In this analysis, the null hypothesis is accepted. The ANOVA shows that the improvement in the number of test sites has no effect on the ROI. Thus, this analysis of ROI for wafer-ring test equipment implies that the improvement in test sites has no effect on the ROI improvement. Therefore, no further post hoc test analysis is required.

VII. CONCLUSIONS

ROITM has a direct relation with the profit and the cost of test. In ROI, the cost is used as the investment, and the test profit is used as the profit for the ROI, where the ROI is derived as the profit over investment. The ROI analysis shows that the increment in test sites does not directly contribute to the improvement in the ROI rate. The main reason is that the increment in test sites does not reflect a significant improvement in the throughput while the investment in multi-sites increases. The test throughput is the main contributor to improved profits because of the fixed cost. A high throughput leads to a reduced cost per unit and therefore an improved profit margin. The profit directly contributes to the ROI. If the profit does not improve significantly, then the ROI rate also does not improve significantly.

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Khoo Voon Ching" A Case Study of Return on Investment in Wafer-Ring Multi-sites Test Handler for the Semiconductor Industry Paper" American Journal of Engineering Research (AJER), vol. 8, no. 10, 2019, pp 58-76